SYED AMMAL ENGINEERING COLLEGE

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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TWO MARKS – QUESTION BANK

UNIT I – MOS TRANSISTOR PRINCIPLE

1. What is Moore's law?

Moore's law states that the number of transistor would double every 18 months

2. What is CMOS technology?

Complementary Metal Oxide Semiconductor (CMOS)in which both n-channel MOS and p-channel MOS are fabricated in the same IC.

3. What are the advantages of CMOS over NMOS technology ?

1. In CMOS technology the aluminum gates of the transistor are replaced by poly silicon gate.
2. The main advantage of CMOS over NMOS is low power consumption.
3. In CMOS technology the device sizes can be easily scalable than NMOS.

4. What are the advantages of CMOS technology?

1. Low power consumption.
2. High performance.
3. Scalable threshold voltage.
4. High noise margin.
5. Low output drive current

5. What are the disadvantages of CMOS technology?

1. Low resistance to produce deviations and temperature changes.
2. Low switching speed at large values of capacitive loads.

6. What is design rule?

Design rules are the communication link between the designer specifying requirements and the fabricator who materializes them. The design rule conform to a set of geometric constraints or rule specify the minimum allowable line widths for physical objects on-chip such as metal and poly silicon Interconnects or diffusion area, minimum feature dimensions and minimum allowable separations between two layers.

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7. What is stick diagram?

Stick diagram are the key element of designing a circuit used to convey layer information through the use of a color code.

8. What is micron design rule?

Micron rules specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometres.

9. What is Lambda design rule?

Lambda rule specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of a single parameter (λ) and thus allow linear, proportional scaling of all geometrical constraints.

10. What is DRC?

Design Rule Check program looks for design rule violations in the layout. It checks for minimum spacing and minimum size and ensures that combinations of layers from legal components.

11. Mention MOS transistor characteristics?

- Metal Oxide Semiconductor is a three terminal device having source, drain and gate.
- The resistance path between the drain and the source is controlled by applying a voltage to the gate.
- The Normal conduction characteristics of an MOS transistor can be categorized as cut-off region, non- saturated region and saturated region.

12. Compare NMOS and PMOS ?

NMOS	PMOS
The majority carriers are electrons	The majority carriers are holes
Positive voltage is applied at the gate terminal	Negative voltage is applied at the gate terminal
NMOS conducts at logic 1	PMOS conducts at logic 0
Mobility of electron is high	Mobility of electron is low
Switching speed is high	Switching speed is low

13. Compare enhancement and depletion mode devices?

Enhancement	**Depletion**
1. No conducting channel between source and drain unless a positive voltage is applied	Channel exists even with zero voltage from gate to source. In order to control the

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	channel a negative voltage is applied to the gate
2. Enhancement-mode device is equivalent to a normally open (off)switch	Depletion-mode device is equivalent to a normally closed (on)switch

14. What is threshold voltage?
It is defined as the minimum voltage at which the device starts conduction (ie) turns on.

15. What are different operating modes of MOS transistor?
- Accumulation mode
- Depletion mode
- Inversion mode

16. What is accumulation mode?
When the gate to source voltage(Vgs) is much less than the threshold voltage (Vt) then it is termed as the accumulation mode. There is no conduction between source and drain. The device is turned off.

17. What is depletion mode?
When the gate to source voltage(Vgs) is increased greater than the threshold voltage (Vt) the electrons are attracted towards the gate while the holes are repelled causing a depletion region under the gate. This is called depletion mode.

18. What is inversion mode?
When Vgs is raised above the Vt the electrons are attracted to the gate region. Under such a condition the surface of the underlying p-type silicon is said to be a inverted to n-type, and provides a conduction path between a source and drain. The device is turned on. This is called inversion mode.

19. What are three operating regions of MOS transistor?
- Cut-off region
- Non saturated region
- Saturated region

20. What is cut-off region?
The region where the current flow is essentially zero is called cut-off region.
(ie) Ids=0, Vgs ≤ Vt.

21 What is Non-saturated region?
Weak inversion region where the drain current is dependent on the gate and the drain voltage is called non saturated region

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(ie) 0<Vds < Vgs – Vt

22. What is saturated region?
Channel is strongly inverted and the drain current flow is ideally independent of the drain-source voltage is called saturated region.
(ie) 0 < Vgs – Vt< Vds

23. What is body effect? Write the threshold voltage equation including the body effect?
The threshold voltage Vt is constant with respect to voltage difference between source and the substrate is called body effect.
$Vt = Vfb + 2\varphi b + \sqrt{2\varepsilon qNa(2\varnothing b + Vsb)} / Cox$

24. Define threshold voltage for a MOSFET?
The threshold voltage of a MOSFET is usually defined as the gate voltage were an inversion layer form at the interface between the insulating layer (oxide) and the substrate (body) of the transistor.

25. What is body effect in MOSFETs?
The body effect is change in the threshold voltage by the change in the VSB(the source bulk voltage). Since the body influences the threshold voltage (when it is not tied to the source), it can be considered as second gate or back gate. For enhancement mode , the n-mos MOSFET body effect upon threshold voltage is given as
$Vtn = Vto + \gamma (\sqrt{Vsb + 2\varnothing f} - \sqrt{2\varnothing f})$
Where, Vtn is threshold voltage when substrate is present,
Vsb is the source to body substrate bias,
2ϕf is the source potential and
Vto is the threshold voltage for zero substrate bias.

26. What is the objective of layout rules ?
- To build reliably functional circuits in as small an area as possible.
- To provide a necessary communication link circuit designer and process engineer during manufacturing.
- To obtain a circuit with optimum yield in smallest possible area.

PART –B
1. Discuss in detail with a neat layout, the design rules for a CMOS inverter.
2. Discuss in detail with necessary equation the operation of MOSFET and its current voltage characteristics.
3. Draw and explain the D.C and transfer characteristics of a CMOS inverter with a necessary conditions for the different regions of operation.
4. Discuss the principle of constant field scaling and also write its effect on device characteristics.
5. Explain the small signal model of MOS transistors with neat diagram and expression.

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6. Draw the stick diagram and layout of a NMOS and CMOS inverter.

UNIT 2 - COMBINATIONAL LOGIC CIRCUITS

PART A

1. Define Elmore delay model?
It is an analytical method used to estimate the RC delay in a network. Elmore delay model estimates the delay of a RC ladder as the sum over each node in the ladder of the resistance Rn-1 between that node and a supply multiplied by the capacitor on the nodes.

2. What are the general properties of Elmore delay model?
General property of Elmore delay model network has
- Single input node
- All the capacitors are between a node and ground
- Network does not contain any resistive loop

3. What are the types of power dissipation?
- Static power dissipation (due to leakage current when the circuit is idle).
- Dynamic power dissipation (when the circuit is switching) and
- Short –circuit power dissipation during switching of transistors.

4. What is static power dissipation?
Power dissipation due to leakage current when the idle is called the static power dissipation. Static power due to
- Sub – threshold conduction through OFF transistors
- Tunnelling current through gate oxide
- Leakage through reverse biased diodes
- Contention current in radioed circuits.

5. What is Dynamic power dissipation?
Power dissipation is due to circuit switching to charge and discharge the output load capacitance at a particular node at operating frequency is called Dynamic power dissipation. The Dynamic power dissipation at a particular output node is given by
Pd=CL Vdd^2 Fclk.a ; where, CL = load capacitance ; a = activity factor ;Vdd =power supply ; Fclk= operating frequency

6. What are the methods to reduce dynamic power dissipation?
1. Reducing the product of capacitance and its switching frequency.
2. Eliminate logic switching that is not necessary for computation.
3. Reduce activity factor Reduce supply voltage

7. What are the methods to reduce static power dissipation?

1. By selecting multi threshold voltages on circuit paths with low-Vt transistors while leakage on other paths with high-Vt transistors.
2. By using two operating modes, active and standby for each function blocks.
3. By adjusting the body bias (i.e) adjusting FBB (Forward Body Bias) in active mode to increase performance and RBB (Reverse Body Bias) in standby mode to reduce leakage.
4. By using sleep transistors to isolate the supply from the block to achieve significant leakage power savings.

8. What is short circuit power dissipation?

During switching, both NMOS and PMOS transistors will conduct simultaneously and provide a direct path between Vdd and the ground rail resulting in short circuit power dissipation.

9. Define design margin?

The additional performance capability above required standard basic system parameters that may be specified by a system designer to compensate for uncertainties is called design margin. Design margin required as there are three sources of variation- two environmental and one manufacturing.

10. Write the applications of transmission gate?

Multiplexing element of path selector
A latch element An unlock switch
Act as a voltage controlled resistor connecting the input and output.

11. What is pass transistor?

It is a MOS transistor, in which gate is driven by a control signal the source (out), the drain of the transistor is called constant or variable voltage potential (in) when the control signal is high, input is passed to the output and when the control signal is low, the output is floating topology such topology circuits is called pass transistor.

12. List the advantages of pass transistor?

Pass transistor logic (PTL) circuits are often superior to standard CMOS circuits in terms of layout density, circuit delay and power consumption.
They do not have path VDD to GND and do not dissipate standby power(static power dissipation).

13. What is transmission gate?

The circuit constructed with the parallel connection of PMOS and NMOS with shorted drain and source terminals. The gate terminal uses two select signals s and s, when s is high than the transmission gates passes the signal on the input. The main advantage of transmission gate is that it eliminates the threshold voltage drop.

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14. Why low power has become an important issue in the present day VLSI circuit realization?
In deep submicron technology the power has become as one of the most important issue because of:
1. Increasing transistor count; the number of transistor is getting doubled in every 18 months based on Moore's law.
2. Higher speed of operation: the power dissipation is proportional to clock frequency
3. Greater device leakage current: in nano-meter technology the leakage component become a significant percentage of the total ower and the leakage current increases at a faster rate then dynamic power in technology generations.

15. What are the various ways to reduce the delay time of a CMOS inverter?
Various ways for reducing the delay time are given below:

a) The width of the MOS transistor can be increased to reduce delay. This is known as gate sizing,

b) The load capacitance can be reduced to reduce delay. This is achieved by using transistor of smaller and smaller dimension by feature generation technology.

c) Delay can also be reduced by increasing the supply voltage Vdd and/or reducing the threshold voltage Vt of the MOS transistors

16. Explain the basic operation of a 2- phase dynamic circuit?
The operation of the circuit can be explained using pre-charge logic in which the output is pre-charged to HIGH level during Φ2 clockand the output is evaluated during Φ1 clock.

17. What makes dynamic CMOS circuits faster than static CMOS circuits?
As MOS dynamic circuits require lesser number of transistor and capacitance is to be driven by it. This makes MOS dynamic circuits faster.

18. What is glitching power dissipation?
Because of finite delay of the gates used to realize boolean functions,different signals cannot reach the inputs of a gate simultaneously.this leads to spurious transition at the output before it settles down to its final value.the spurious transitions leads to charging and discharging of the outputs causing glitching power dissipation. It can be minimized by having balanced realization having same delay at the inputs.

19. List various sources of leakage currents?
Various source of leakage currents are listened below:

I1=Reverse-bias p-n junction diode leakage current.
I2=band-to-band tunneling current
I3=Subthreshold leakage current
I4=Gate oxide tunneling current
I5=Gate current due to hot carrier junction

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I6=Channel punch through
I7=Gate induced drain leakage current

20. Compare and contrast clock gating versus power gating approaches.
Clock gating minimizes dynamic power by stopping unnecessary transitions, but power gating minimizes leakage power by inserting a high Vt transistor in series with low Vt logic blocks.

PART – B

1. Discuss in detail about the ratioed circuit and dynamic circuit CMOS logic configurations
2. Describe the basic principle of operation of dynamic CMOS, domino and NP domino logic with neat diagrams.
3. Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions.
4. Discuss the design techniques to reduce switching activity in a static and dynamic CMOS circuits.
5. Briefly discuss about the classification of circuit families and comparison of circuit families.

UNIT -3
SEQUENTIAL LOGIC CIRCUITS
PART – A

1. What are the classification of CMOS circuit families?
   Static CMOS circuits.
   Dynamic CMOS circuits.
   Ratioed circuits.
   Pass-transistor circuits.

2. What is the characteristics of Static CMOS design?
A static CMOS circuit is a combination of two networks – the pull-up network (PUN) and the pull-down network (PDN) in which at every point in time, each gate output is connected to either VDD or VSS via a low resistance line.

3. List the important properties of Static CMOS design?
   a. The function of the PUN is provide a connection between the output and VDD.
   b. The function of the PDN is provide a connection between the output and VSS .
   c. Both PDN and PUN are constructed in mutually exclusive way such that one and only one of the networks is conducting in steady state. That is, the output node is always a low-impedance node in steady state.

4. What is Dynamic CMOS logic?

Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance node.

Requires only N+2 transistors.

Takes a sequence of precharge and conditional evaluation phases to realizes logic functions.

5. What are the properties of Dynamic logic?

Logic function is implemented by pull-down network only.
Full swing outputs (VOL= GND and VOH = VDD).
Non-ratioed.
Faster switching speeds.
Needs a precharge clock.

6. What are the disadvantages of dynamic CMOS technology?

a. A fundamental difficulty with dynamic circuits is a loss of noise immunity and a serious timing restriction on the inputs of the gate.
b. Violate monotonicity during evaluation phase.

7. What is CMOS Domino logic?

A static CMOS inverter placed between dynamic gates which eliminate the monotonicity problem in dynamic circuits are called CMOS Domino logic.

8. What is called static and dynamic sequencing element?

1. A sequencing element with static storage employs some sort of feedback to retain its output value indefinitely.
2. A sequencing element with dynamic storage generally maintain its value as charge on a capacitor that will leak away if not refreshed for a long period of time.

9. What is clock skew?

In reality clocks have some uncertainty in their arrival times that can cut into the time available for useful computation is called clock skew.

10. What are synchronizers?

Synchronizers are used to reduce meta-stability. The synchronizers ensure synchronization between asynchronous input and synchronous system.

11. What is the difference between Mealy and Moore state machines?

In the Mealy state machine we can calculate the next state and output both from the input and state. But in the moore state machine we can calculate only next state but not output from the input and the state and the output is issued according to next state.

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12. Define propagation delay and contamination delay?

Propagation delay(t pd): The amount of time needed for a change in a logic input to result in a permanent change at an output,that is the combinational logic will not show any further output changes in response to an input change alter time fod units contamination delay(tea): The amount of time needed for a change in a logic input to result in an initial change at an output, that is the combinational logic is guaranteed not to show any output change in response to an input change before fed time units have passed.

13. Define Setup time and Hold time.

Setup time (t setup): The amount of time before the clock edge that data input D must be stable the rising clock edge arrives.

Hold time (t hold): This indicates the amount of time after the clock edge arrives the data input D must be held stable in order for FF to latch the correct value. Hold time is always measured from the rising clock edge to a point after the clock edge.

14. Difference between latches and Flip-Flop.

Latch	Flip-Flop
A Latch is Level-Sensitive	A FF is edge triggered.
A latch stores when the clock level is low and is transparent when the level is high.	A FF stores when the clock rises and is mostly never transparent.

15. Define Pipelining.

Pipelining is a popular design technique often used to accelerate the operation of the data path in digital processors. The major advantages of pipelinig are to reduce glitching in complex logic networks and getting lower energy due to operand isolation.

16. How the limitations of a ROM-based realization is overcome in a PLA-based realization.

In a ROM, the encoder part is only programmable and use of ROMs to realize Boolean functions is wasteful in many situations because there is no cross-connect for a significant part. This wastage can be overcome by using Programmable Logic Array (PLA), which requires much lesser chip area.

17. In what way the DRAMs differ from SRAMs?

Both SRAMs and DRAMs are volatile in nature, ie. Information is lost if power line is removed. However SRAMs provide high switching speed, good noise margin but require large chip area than DRAMs.

18. Explain the read and write operations for a one-transistor DRAM cell.

A significant improvement in the DRAM evolution was to realize 1-T DRAM cell. One additional capacitor is explicitly fabricated for storage purpose. To store 'I', it is charged to store '0' it is

discharged to '0' volt. Read operation is destructive. Sense amplifier is needed for reading. Read operation is followed by restoration operation.

19. What do you meant by Min delay constraint?
Min delay constraint: the path begins with the rising edge of the clock triggering F1. The data may begin to change at Q1 after a clk-to-Q contamination delay. However, it must not reach D2 until at least the hold after the clock edge, lest it corrupt the contents of F2. Hence, we solve for minimum logic contamination delay:
tcd >= thold – tccq

20. What do you meant by Max delay constraint?
Max delay constraint: the path begins with the rising edge of the clock triggering F1. The data must propagate to the output of the flipflop Q1 and through the combinational logic to D2, setting up at F2 before the next rising clock edge. Under ideal conditions, the worst case propagation delays determine the minimum clock period for this sequential circuitry.
Tc >= tpcq + tpd + tsetup

PART – B

1. Write a brief note on sequencing dynamic circuits.
2. Explain in detail about the principle concepts used in sequential circuits.
3. How do you achieve low power in memory circuits? Explain in detail.
4. Discuss in detail about dynamic RAM.
5. Illustrate the principles of synchronizer and arbiter.

UNIT – 4
DESIGNING ARITHMETIC BUILDING BLOCK
PART – A

1. How path can be implemented in VLSI system?
A data path is best implemented in a bit –sliced fashion. A single layout is used respectively for every bit in the data word. This regular approach eases the design effort and results in fast and dense layouts.

2. Comment on performance of ripple carry adder.
A ripple carry adder has a performance that is linearly proportional to the number of bits. Circuit optimizations concentrate on reducing the delay of the carry path. A number of circuit topologies exist providing that careful optimization of the circuit topology and the transistor sizes helps to reduce the capacitance on the carry bit.

3. What is the logic of adder for increasing its performance?

Other adder structures use logic optimizations to increase the performance (carry bypass, carry select, carry look ahead). Performance increase comes at the cost area.

4. What is multiplier circuit?
A multiplier is nothing more than a collection of cascaded adders. Critical path is far more complex and optimizations are different compared to adders.

5. Which factors dominate the performance of programmable shifter?
The performance and the area of a programmable shifter are dominated by the wiring.

6. What is meant by data path?
A data-path is a functional units, such as arithmetic logic units or multipliers that perform data processing operations, registers and buses. Along with the control unit it composes the central processing unit.

7. Write down the expression for worst-case delay for RCA.

$t = (n-1)tc+ts$

8. Write down the expression to obtain delay for N-bit carry bypass adder.

$tadder = tsetup + Mtcarry + (N/M-1)tbypass + (M-1)tcarry + tsum$

9. Define Braun multiplier.
The simplest multiplier is the Braun multiplier. All the partial products are computed in parallel, and then collected through a cascade of Carry Save Adders. The completion time is limited by the depth of the carry save array, and by the carry propagation in the adder. This multiplier is suitable for positive operands.

10. Why Booth's algorithm is said to be effective?
Booth algorithm is a method that will reduce the number of multiplicand multiples. For a given number of ranges to be represented, a higher representation radix leads to fewer digits.

11. List the different types of shifter.
- Array shifter
- Barrel shifter
- Logarithm shifter

PART – B

1. Explain the structure of booth multiplier and list its advantages.
2. Design a 3 bit barrel shifter
3. What is 4*4 carry save multiplier. Calculate its critical path delay

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4. Explain the following circuits 1. Data path circuit 2. Any one adder circuit
5. Explain with neat diagram baugh-wooley multiplier
6. Explain ripple carry adder.
7. Describe about carry look-ahead adder and its carry generation and propagation.

UNIT – 5
IMPLEMENTATION STRATEGIES
PART – A

1. Differentiate between channelled and channel less gate array.

Channelled gate array	Channel less gate array
Only the interconnect is customized	Only the top few mask layers are customized
The interconnect uses predefined spaces between rows of base cells.	No predefined areas are set aside for routing between cells.
Routing is done using spaces.	Routing is done using the area of transistors unused
Logic density is less.	Logic density is higher.

2. What are the different levels of design abstraction at physical design?
   - Architectural or functional unit
   - Register Transfer-level (RTL)
   - Logic level
   - Circuit level

3. What are macros?
The logic cells in a gate-array are often called macros.

4. What are programmable Interconnects?
In a PAL, the device is programmed by changing the characteristics if the switching element. An alternative would be to program the routing.

5. What are the types of ASICs?
Types of ASICs are
   - Full custom ASICs
   - Semi-custom ASICs

6. What are the types of programmable devices?
   - Types of programmable devices are
     - Programmable logic structure

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Programmable Interconnect
Reprogrammable Gate Array

7. What are the features of standard celled ASICs?
   All mask layers are customized-transistors and interconnect.
   Custom blocks can be embedded
   Manufacturing lead time is about eight weeks.

8. What are the characteristics of FPGA?
   None of the mask layers are customized
   A method of programming the basic logic cells and interconnect.
   The core is a array of programmable basic logic cells that can implement combinational as well as sequential logic (flipflops).
   A matrix of programmable interconnect surrounds the basic logic cells.
   Design turnaround is a few hours.

9. What is programmable logic array?
A programmable logic array (PLA) is a programmable device used to implement combinational logic circuits. The PLA has a set of programmable AND planes, which link to a programmable OR planes, which can then be conditionally complemented to produce an output. This layout allows for a large number of logic functions to be synthesized in the sum of products (sometimes product of sums) canonical forms.

10. What is meant by programmable logic plane?
The programmable logic plane is programmable read only memory (PROM) array that allows the signals present on the devices pins to be routed to an output logic macro cell.

11. Give the application of PLA.
   Design and testing of digital circuits.

12. Give the different types of ASIC.
   1. Full custom ASICs
   2. Semicustom ASICs
      Standard cell based ASICs
      Gate-array based ASICs
   3. Programmable ASICs
      Programmable Logic Device (PLD)
      Field Programmable Gate Array (FPGA).

13. What is the full custom ASIC design?

In a Full custom ASIC, an engineer designs some or all of the logic cells, circuits or layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

14. What is standard cell-based ASIC design?

A cell-based ASIC (CBIC) uses predefined logic cells known as STANDARD CELLS. The standard cell areas are also called flexible block in a CBIC are built of rows of standard cells. The ASIC designer defines only the placement of standard cells and interconnect in a CBIC. All the mask layers of a CBIC are customized and are unique to a particular customer.

15. What is FPGA?

A Field Programmable Gate Array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGA can be used to implement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of upto about 20,000 equivalent gates.

16. What are the different methods of programming of PALs?

The programming of PALs in done in three ways:

1. Fusible links
2. UV-erasable EPROM
3. EEPROM(E2PROM) – Electrically Erasable Programmable ROM.

17. What is an anti-fuse?

An antifuse is normally high resistance (>100MΩ). on application of appropriate programming voltages, the antifuse is changed permanently to a low-resistance structure(200- 500Ω) .

18. Give the steps in ASIC design flow?

1. Design entry
2. Logic synthesis system partitioning
3. Prelayout simulation
4. Floor planning
5. Placement
6. Routing
7. Extraction
8. Post layout simulation

PART – B

1. Explain the general architecture of FPGA and bring about different programmable blocks used.
2. Discuss in detail about full custom design and semi-custom design.
3. Describe about Gate-Array Based ASICs.
4. Write short note on programmable Logic Devices.

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5. Write short notes on standard cell design and cell libraries.
6. Write the significance of PLA/FSM in VLSI design.
7. Explain the programmable interconnects and I/O blocks used in FPGA.

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