SYED AMMAL ENGINEERING COLLEGE, RAMANATHAPURAM

An Autonomous Institution & Affiliated to Anna University Chennai

REGULATION 2024

CHOICE BASED CREDIT SYSTEM

M.E VLSI DESIGN ENGINEERING

VISION	MISSION
To contribute the quality Engineers to the society by making students powerful and employable in Electronics, Communication and Computer technologies	• To enhance the quality of education in Electronics and Communication Engineering • To empower the rural students to gain innovative ideas by inculcating them with curricular and co-curricular activities • To train the students in developing intellectual excellence with ethical values to meet the global challenges.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)
Graduates of M.E. VLSI Design Engineering shall:
PEO1: To prepare the graduates to excel in industry and to motivate for higher education by educating graduates along with high moral values and knowledge.
PEO2: To encourage the graduates in developing their competency in the field of Signal processing, Embedded systems, VLSI and Wireless communication technologies.
PEO3: To train graduates with good engineering breadth so as to comprehend, analyze, design and create novel products and solutions for the real life problems.
PE04: To inculcate professional and ethical attitude, effective communication skills, team work skills, multi-disciplinary approach, entrepreneurial thinking and an ability to relate engineering issues to broader social context in graduates.
PE05: To provide graduates with an academic environment aware of excellence, leadership, written ethical codes and guidelines and the self-motivated lifelong learning needed for a successful professional career.
PROGRAM OUTCOMES (POs)
M.E VLSI Design Engineering Graduates will be able to

PO1: An ability to independently carry out research/investigation and development work to solve practical problems
PO2: An ability to write and present a substantial technical report/document
PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program The mastery should be at a level higher than the requirements in the appropriate bachelor program
PO4: Understand the fundamentals involved in the Designing and Testing of electronic circuits in the VLSI domain.
PO5: Provide solutions through research to socially relevant issues for modern Electronic Design Automation (EDA) tools with knowledge, techniques, skills and for the benefit of the society
PO6: Interact effectively with the technical experts in industry and society.

PEO/PO Mapping:

PEO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
I	✓	✓	✓	✓	✓	✓
II	✓	✓	✓	✓	▪	▪
III	✓	▪	✓	▪	✓	✓
IV	▪	✓	▪	▪	▪	✓
V	✓	✓	✓	✓	✓	✓

MAPPING OF COURSE OUTCOMES AND PROGRAMME OUTCOMES

		COURSE NAME	PO1	PO2	PO3	PO4	PO5	PO6
YEAR I	SEMESTER I	Graph Theory and Optimization Techniques	2	0	1	1	0	0
		Research Methodology and IPR	2	2	-	-	2	-
		Analog IC Design	1	1	2	1	2	0
		Digital CMOS VLSI Design	1	0	1.4	1	0	0
		Advanced Digital System Design	1	0	1	1	1.2	0
		Semiconductor Devices and Modeling	2	0	1.4	1	2	0
		FPGA Laboratory	1	1	1	1	1	1
		Analog IC Design Laboratory	1	1	1	1	2	1
	SEMESTER II	Design for Verification using UVM	1	0	1	1	2.5	0
		Low Power VLSI Design	1.6	0	2	2.4	2.2	0
		RFIC Design	1.6	0	2	2.2	2	0
		VLSI Testing	1.6	0	2	2.4	2.4	1
		Professional Elective I						
		Professional Elective II						
		Verification using UVM Laboratory	1	3	1	1	1	3
		Term Paper and Seminar	1	1	1	1	1	1
YEAR II	SEMESTER Iii	VLSI Signal Processing	1	0	1	1	0	0
		Professional Elective III						
		Professional Elective IV						
		Open Elective						
		Project Work I						
	SEMESTER IV	Project Work II						

PROFESSIONAL ELECTIVE COURSES [PEC]

S.NO.	COURSE NAME	PO1	PO2	PO3	PO4	PO5	PO6
1	ASIC Design	1	0	2	2	1	0
2	Embedded System Design	1	0	2	2	3	1
3	Electromagnetic Interference and Compatibility	2.5		1	2	1	1
4	Data Converters	1	0	2	2	0	0
5	Hardware Software Co-Design for FPGA	1	0	2	2	0.8	0
6	Pattern Recognition	3	0	2	3	1	1
7	DSP Structures for VLSI	1	0	1	1	0	0
8	Power Management and Clock Distribution Circuits	1	0	2	2	0	0
9	Reconfigurable Architectures	1.2	0	2	1.2	0	0
10	Advanced Wireless Sensor Networks	3	0	2	1	3	0
11	Signal Integrity for High Speed Design	1	0	2	2.2	1	0
12	System On Chip	1	0	2	1	0	0
13	MEMS and NEMS	1	0	2	1	2	0
14	Network on Chip	1	0	2	1	3	0
15	Nanotechnology	1	0	1	1	0	0
16	Evolvable Hardware	1	0	2.2	1.2	0	0
17	Soft Computing and Optimization Techniques	1	0	2	1	2	0
18	CAD for VLSI Design	1	0	1	2	2	1
19	VLSI Architectures for Image Processing	1	0	1	1	1	0
20	System Verilog	1	0	2	2	2	1
21	Adaptive Signal Processing	1.6	1	1.6	1.2	1	1
22	Machine Learning	3	0	2	3	1	1
23	Digital Image and Video Processing	3	0	2	2	2	2

SYED AMMAL ENGINEERING COLLEGE, RAMANATHAPURAM – 623502.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E. VLSI DESIGN REGULATIONS – 2024

CHOICE BASED CREDIT SYSTEM

I TO IV SEMESTERS CURRICULA AND I-II SEMESTERS SYLLABI

SEMESTER I

S.NO	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDIT
				L	T	P		
THEORY								
1	24MA003T	Graph Theory and Optimization Techniques	FC	3	1	0	4	4
2	24RM101T	Research Methodology and IPR	RMC	2	0	0	2	2
3	24VL101T	Analog IC Design	PCC	3	0	0	3	3
4	24VL102T	Digital CMOS VLSI Design	PCC	3	0	0	3	3
5	24VL103T	Semiconductor Devices and Modeling	PCC	3	0	0	3	3
6		Audit Course – I*	AC	2	0	0	2	0
THEORY WITH PRACTICAL								
7	24VL101I	Advanced Digital System Design	PCC	3	0	2	5	4
PRACTICALS								
8	24VL101P	FPGA Laboratory	PCC	0	0	4	4	2
9	24VL102P	Analog IC Design Laboratory	PCC	0	0	4	4	2
TOTAL				**19**	**1**	**10**	**30**	**23**

*Audit course is optional

SEMESTER II

S.NO	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDIT
				L	T	P		
THEORY								
1	24VL201T	Design for Verification using UVM	PCC	3	0	0	3	3
2	24VL202T	Low Power VLSI Design	PCC	3	0	0	3	3
3	24VL203T	RFIC Design	PCC	3	0	0	3	3
4	24VL204T	VLSI Testing	PCC	3	0	0	3	3
5		Professional Elective I	PEC	3	0	0	3	3
6		Professional Elective II	PEC	3	0	0	3	3
7		Audit Course – II*	AC	2	0	0	2	0
PRACTICALS								
8	24VL201P	Verification using UVM Laboratory	PCC	0	0	4	4	2
9	24TM201P	Term Paper Writing and Seminar	EEC	0	0	2	2	1
TOTAL				**20**	**0**	**6**	**26**	**21**

*Audit course is optiona

PROFESSIONAL ELECTIVES

SEMESTER II, ELECTIVE I

S.NO	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDIT
				L	T	P		
THEORY								
1	24VL101E	ASIC Design	PEC	3	0	0	3	3
2	24VL102E	Embedded System Design	PEC	3	0	0	3	3
3	24VL103E	Electromagnetic Interference and Compatibility	PEC	3	0	0	3	3
4	24VL104E	Data Converters	PEC	3	0	0	3	3
5	24VL105E	Hardware Software Co- Design for FPGA	PEC	3	0	0	3	3
6	24VL106E	Pattern Recognition	PEC	3	0	0	3	3

SEMESTER II, ELECTIVE II

S.NO	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	TOTAL CONTACT PERIODS	CREDIT
Theory								
1	24VL201E	DSP Structures for VLSI	PEC	3	0	0	3	3
2	24VL202E	Power Management and Clock Distribution Circuits	PEC	3	0	0	3	3
3	24VL203E	Reconfigurable Architectures	PEC	3	0	0	3	3
4	24VL204E	Advanced Wireless Sensor Networks	PEC	3	0	0	3	3
5	24VL205E	Signal Integrity for High Speed Design	PEC	3	0	0	3	3
6	24VL206E	System On Chip	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE III

S.NO	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	TOTAL CONTACT PERIODS	CREDIT
Theory								
1		MEMS and NEMS	PEC	3	0	0	3	3
2		Network on Chip	PEC	3	0	0	3	3
3		Nanotechnology	PEC	3	0	0	3	3
4		Evolvable Hardware	PEC	3	0	0	3	3
5		Soft Computing and Optimization Techniques	PEC	3	0	0	3	3
6		CAD for VLSI Design	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE IV

S.NO	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	TOTAL CONTACT PERIODS	CREDIT
Theory								
1		VLSI Architectures for Image Processing	PEC	3	0	2	5	4
2		System Verilog	PEC	3	0	2	5	4
3		Adaptive Signal Processing	PEC	3	0	2	5	4
4		Machine Learning	PEC	3	0	2	5	4
5		Digital Image and Video Processing	PEC	3	0	2	5	4

AUDIT COURSES (AC)

Registration for any of these courses is optional to students

S.NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDIT
			L	T	P	
1		English for Research Paper Writing	2	0	0	0
2		Disaster Management	2	0	0	0
3		Constitution of India	2	0	0	0
4		நற்றமிழ் இலக்கியம்	2	0	0	0

LIST OF OPEN ELECTIVES FOR PG PROGRAMMES

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDIT
			L	T	P	
1		Integrated Water Resources Management	3	0	0	3
2		Water, Sanitation and Health	3	0	0	3
3		Principles of Sustainable Development	3	0	0	3
4		Environmental Impact Assessment	3	0	0	3
5		Blockchain Technologies	3	0	0	3
6		Deep Learning	3	0	0	3
7		Vibration and Noise Control Strategies	3	0	0	3
8		Energy Conservation and Management in Domestic Sectors	3	0	0	3
9		Additive Manufacturing	3	0	0	3
10		Electric Vehicle Technology	3	0	0	3
11		New Product Development	3	0	0	3
12		Sustainable Management	3	0	0	3
13		Micro and Small Business Management	3	0	0	3
14		Intellectual Property Rights	3	0	0	3
15		Ethical Management	3	0	0	3
16		IoT for Smart Systems	3	0	0	3
17		Machine Learning and Deep Learning	3	0	0	3
18		Renewable Energy Technology	3	0	0	3
19		Smart Grid	3	0	0	3
20		Security Practices	3	0	0	3
21		Cloud Computing Technologies	3	0	0	3

22		Design Thinking	3	0	0	3
23		Principles of Multimedia	3	0	0	3
24		Environmental Sustainability	3	0	0	3
25		Textile Reinforced Composites	3	0	0	3
26		Nanocomposite Materials	3	0	0	3
27		IPR, Biosafety and Entrepreneurship	3	0	0	3

FOUNDATION COURSES (FC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDIT	SEMESTER
			L	T	P		
1		Graph Theory and Optimization Techniques	3	1	0	4	I

PROFESSIONAL CORE COURSES (PCC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDIT	SEMESTER
			L	T	P		
1		Analog IC Design	3	0	0	3	I
2		Digital CMOS VLSI Design	3	0	0	3	I
3		Advanced Digital System	3	0	2	4	I
4		Semiconductor Devices and Modeling	3	0	0	3	I
5		FPGA Laboratory	0	0	4	2	I
6		Analog IC Design Laboratory	0	0	4	2	I
7		Design for Verification using UVM	3	0	0	3	II
8		Low Power VLSI Design	3	0	0	3	II
9		RFIC Design	3	0	0	3	II
10		VLSI Testing	3	0	0	3	II
11		Verification using UVM Laboratory	0	0	4	2	II
12		VLSI Signal Processing	3	0	0	3	III

RESEARCH METHODOLOGY AND IPR COURSES (RMC)

S.NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDIT	SEMESTER
			L	T	P		
1		Research Methodology and IPR	2	0	0	2	1

EMPLOYABILITY ENHANCEMENT COURSES (EEC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDIT	SEMESTER
			L	T	P		
1		Mini Project with seminar	0	0	2	1	II
2		Project Work I	0	0	12	6	III
3		Project Work II	0	0	24	12	IV

SUMMARY

Sl. No.	NAME OF THE PROGRAMME: M.E.VLSI DESIGN					
	SUBJECT AREA	CREDITS PER SEMESTER				CREDITS TOTAL
		I	II	III	IV	
1	FC	04	00	00	00	04
2	PCC	17	14	03	00	34
3	PEC	00	06	07	00	13
4	RMC	02	00	00	00	02
5	OEC	00	00	03	00	03
6	EEC	00	01	06	12	19
7	Non Credit/Audit Course			00	00	
8	**TOTAL CREDIT**	**23**	**21**	**19**	**12**	**75**

24MA003T	GRAPH THEORY AND OPTIMIZATION TECHNIQUES	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES:

- To introduce graph as mathematical model to solve connectivity related problems.
- To introduce fundamental graph algorithms.
- To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in a real life situation.
- To provide knowledge and training using non-linear programming under limited resources for engineering and business problems.
- To understand the applications of simulation modelling in engineering problems.

UNIT I GRAPHS 12

Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism – Connectivity – Euler and Hamilton paths.

UNIT II GRAPH ALGORITHM 12

Graph Algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms – Depth – First search on a graph – Theoretic algorithms – Performance of graph theoretic algorithms – Graph theoretic computer languages.

UNIT III LINEAR PROGRAMMING 12

Formulation – Graphical solution – Simplex method – Two-phase method – Transportation and Assignment Models.

UNIT IV NON-LINEAR PROGRAMMING 12

Constrained Problems – Equality constraints – Lagrangean Method – Inequality constraints – Karush – Kuhn-Tucker (KKT) conditions – Quadratic Programming.

UNIT V SIMULATION MODELLING 12

Monte Carlo Simulation – Types of Simulation – Elements of Discrete Event Simulation – Generation of Random Numbers – Applications to Queuing systems.

TOTAL : 60 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to

- apply graph ideas is solving connectivity related problems.
- apply fundamental graph algorithms to solve certain optimization problems.
- formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.
- model various real-life situations as optimization problems and effect their solution through Non-linear programming.
- apply simulation modeling techniques to problems drawn from industry management and other engineering fields.

TEXT BOOKS:

1. Taha H.A, "Operation Research: An Introduction", Ninth Edition, Pearson Education, New Delhi, 2010.
2. Gupta P. K, and Hira D.S., "Operation Research", Revise Edition, S. Chand and Company Ltd., 2012.
3. Sharma J.K., "Operation Research", 3rd Edition, Macmillan Publishers India Ltd., 2009.
4. Douglas B. West, "Introduction to Graph Theory", Pearson Education, New Delhi, 2015.
5. Balakrishna R., Ranganathan. K., " A text book of Graph Theory", Springer Science and Business

Media, New Delhi, 2012.
6. Narasingh Deo, "Graph Theory with Applications to Engineering and Computer Science", Prentice Hall India,1997.

CO-PO MAPPING:

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	2	0	1	1	0	0
2	2	0	1	1	0	0
3	2	0	1	1	0	0
4	2	0	1	1	0	0
5	2	0	1	1	0	0
Avg	(10/5)=2	0	(5/5)=1	(5/5)=1	0	0

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24RM101T RESEARCH METHODOLOGY AND IPR L T P C
2 0 0 2

COURSE OBJECTIVES:

- To arrange the conditions for collection and analysis of data in a manner that aims to combine relevance to the research purpose
- To gather information in a measured and systematic manner to ensure accuracy and facilitate data analysis
- To transform and model the collected data to discover useful information for decision- making
- To create public awareness about the benefits of Intellectual property among students
- To Provide legal certainty to inventors/ Patent applicants

UNIT I RESEARCH DESIGN 6

Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys.

UNIT II DATA COLLECTION AND SOURCES 6

Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods. Data - Preparing, Exploring, examining and displaying.

UNIT III DATA ANALYSIS AND REPORTING 6

Overview of Multivariate analysis, Hypotheses testing and Measures of Association. Presenting Insights and findings using written reports and oral presentation.

UNIT IV INTELLECTUAL PROPERTY RIGHTS 6

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

UNIT V PATENTS 6

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types

of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licences, Licensing of related patents, patent agents, Registration of patent agents.

TOTAL:30 PERIODS

COURSE OUTCOMES:

- Ability to arrange the conditions for collection and analysis of data in a manner that aims to combine relevance to the research purpose
- Ability to gather information in a measured and systematic manner to ensure accuracy and facilitate data analysis
- Ability to transform and model the collected data to discover useful information for decision-making
- Ability to awareness about the benefits of Intellectual property
- Ability to take up legal certainty while applying for Patent

REFERENCES:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, "Business Research Methods", Tata McGraw Hill Education, 11e (2012).
2. Catherine J. Holland, "Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets", Entrepreneur Press, 2007.
3. David Hunt, Long Nguyen, Matthew Rodgers, "Patent searching: tools & techniques", Wiley, 2007.
4. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.

CO-PO MAPPING:

CO	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
1	3	2	-	-	2	-
2	3	3	-	-	1	-
3	2	3	-	-	1	-
4	1	1	-	-	3	-
5	1	1	-	-	3	-
Avg	**2**	**2**	**-**	**-**	**2**	**-**

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL101T ANALOG IC DESIGN L T P C

3 0 0 3

COURSE OBJECTIVES:

- Analog Circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology.
- The most important building blocks of all CMOS analog IC will be the topic of study in this course.
- The basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs will be discussed in this course.
- The specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability will be dealt with in detail.

UNIT I SINGLE STAGE AMPLIFIERS 9

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, differential amplifier with active load, Cascode and Folded Cascode configurations with active load, design of Differential and Cascode Amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.

UNIT II HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS 9

Miller effect, association of poles with nodes, frequency response of CS, CG and Source Follower, Cascode and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers.

UNIT III FEEDBACK AND SINGLE STAGE OPERATIONAL AMPLIFIERS 9

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, single stage Op Amps, two-stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER 9

Analysis Of Two Stage Op Amp – Two Stage Op Amp Single Stage CMOS CS as Second Stage And Using Cascode Second Stage, Multiple Systems, Phase Margin, Frequency Compensation, And Compensation Of Two Stage Op Amps, Slewing In Two Stage Op Amps, Other Compensation Techniques.

UNIT V BANDGAP REFERENCES 9

Current sinks and sources, current mirrors, Wilson current source, Widlar current source, cascode current source, design of high swing cascode sink, current amplifiers, supply independent biasing, temperature independent references, PTAT and CTAT current generation, constant-gm biasing.

COURSE OUTCOMES:

At the end of this course, the students should will be able to:

CO1: Design amplifiers to meet user specifications.

CO2: Analyse the frequency and noise performance of amplifiers.

CO3: Design and analyse feedback amplifiers and one stage op amps.

CO4: Design and analyse two stage op amps.

CO5: Design and analyse current mirrors and current sinks with mos devices.

TOTAL: 45 PERIODS

REFERENCES

1. Behzad Razavi, “Design Of Analog Cmos Integrated Circuits”, Tata Mcgraw Hill, 2001.
2. Willey M.C. Sansen, “Analog Design Essentials”, Springer, 2006.
3. Grebene, “Bipolar And Mos Analog Integrated Circuit Design”, John Wiley & Sons,Inc.,2003.
4. Phillip E.Allen, Douglas R .Holberg, “Cmos Analog Circuit Design”, Oxford University Press, 2nd Edition, 2002.
5. Recorded Lecture Available at http://www.ee.iitm.ac.in/vlsi/courses/ee5320_2021/start
6. Jacob Baker “CMOS: Circuit Design, Layout, And Simulation, Wiley IEEE Press, 3rd Edition, 2010.

CO-PO MAPPING:

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	1	1	2	1		
2	1		2	1		
3	1		2	1	2	
4	1		2	1	2	
5	1		2	1	2	
Avg	(5/5)=1	(1/1)=1	(10/5)=2	(5/5)=1	(6/3)=2	

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL4102T DIGITAL CMOS VLSI DESIGN

L	T	P	C
3	0	0	3

COURSE OBJECTIVES:

- To introduce the transistor level design of all digital building blocks common to all cmos microprocessors, network processors, digital backend of all wireless systems etc.
- To introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures
- To learn all important issues related to size, speed and power consumption.

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 12

MOSFET characteristic under static and dynamic conditions, MOSFET secondary effects, elmore constant , CMOS inverter-static characteristic, dynamic characteristic, power, energy, and energy delay parameters, stick diagram and layout diagrams.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Static CMOS design, different styles of logic circuits, logical effort of complex gates, static and dynamic properties of complex gates, interconnect delay, dynamic logic gates.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static latches and registers, dynamic latches and registers, timing issues, pipelines, clocking strategies, nonbistable sequential circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS 9

Data path circuits, architectures for adders, accumulators, multipliers, barrel shifters, speed, power and area tradeoffs.

UNIT V MEMORY ARCHITECTURES 6

Memory architectures and Memory control circuits: Read-Only Memories, ROM cells, Read- Write Memories (RAM), dynamic memory design, 6 Transistor SRAM cell, sense amplifiers.

TOTAL:45 PERIODS

REFERENCES:

1. N.Weste, K. Eshraghian, " Principles Of Cmos VLSI Design", Addision Wesley, 2nd Edition, 1993.
2. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997.
3. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis And Design",

CO-PO MAPPING:

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	1	-	1	1	-	-
2	1	-	2	1	-	-
3	1	-	1	1	-	-
4	1	-	2	1	-	-
5	1	-	1	1	-	-
Avg	(5/5)=1	-	(7/5)=1.4	(5/5)=1	-	-

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL101I ADVANCED DIGITAL SYSTEM DESIGN L T P C
3 0 2 4

COURSE OBJECTIVES:

- To design asynchronous sequential circuits.
- To learn about hazards in asynchronous sequential circuits.
- To study the fault testing procedure for digital circuits.
- To understand the architecture of programmable devices.
- To design and implement digital circuits using programming tools.

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Circuits and Modelling- State Diagram, State Table, State Table Assignment and Reduction-Design of Synchronous Sequential Circuits Design of Iterative Circuits-ASM Chart and Realization using ASM.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Asynchronous Sequential Circuit – Flow Table Reduction-Races-State Assignment- Transition Table and Problems in Transition Table- Design of Asynchronous Sequential Circuit - Static, Dynamic and Essential hazards – Mixed Operating Mode Asynchronous Circuits – Designing Vending Machine Controller.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault Table Method-Path Sensitization Method – Boolean Difference Method - D Algorithm — Tolerance Techniques – The Compact Algorithm – Fault in PLA – Test Generation - DFT Schemes – Built in Self Test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming Logic Device Families – Designing a Synchronous Sequential Circuit using PLA/PAL – Designing ROM with PLA – Realization of Finite State Machine using PLD – FPGA – Xilinx FPGA - Xilinx 4000.

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types And Operators For Modelling In Verilog HDL - Behavioural Descriptions In Verilog HDL – HDL Based Synthesis – Synthesis Of Finite State Machines– Structural Modelling – Compilation And Simulation Of Verilog Code – Test Bench - Realization Of Combinational And Sequential Circuits Using Verilog – Registers – Counters – Sequential Machine – Serial Adder – Multiplier- Divider – Design Of Simple Microprocessor, Introduction To System Verilog.

TOTAL:45 PERIODS

SUGGESTED ACTIVITIES:

1: Design asynchronous sequential circuits.
2: Design synchronous sequential circuits using PLA/PAL.
3: Simulation of digital circuits in FPGA.
4: Design digital systems with System Verilog.

PRACTICAL EXERCISES: TOTAL: 30 PERIODS

1. Design of Registers by Verilog HDL.
2. Design of Counters by Verilog HDL.
3. Design of Sequential Machines by Verilog HDL.
4. Design of Serial Adders , Multiplier and Divider by Verilog HDL.
5. Design of a simple Microprocessor by Verilog HDL. Mcgraw-Hill, 1998

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Analyse and design synchronous sequential circuits.
CO2: Analyse hazards and design asynchronous sequential circuits.
CO3: Knowledge on the testing procedure for combinational circuit and PLA.
CO4: Able to design PLD and ROM.
CO5: Design and use programming tools for implementing digital circuits of industry standards.

TOTAL:75 PERIODS

REFERENCES:

1. Charles H.Roth jr., “Fundamentals of Logic Design” Thomson Learning,2013.
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
4. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001.
5. Paragk.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002
6. Paragk.Lala “Digital System Design Using PLD” B S Publications,2003.
7. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

CO-PO MAPPING:

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	1	-	1	1	-	-
2	1	-	2	1	-	-
3	1	-	1	1	-	-
4	1	-	2	1	-	-
5	1	-	1	1	-	-
Avg	(5/5)=1	-	(7/5)=1.4	(5/5)=1	-	-

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL103T SEMICONDUCTOR DEVICES AND MODELING

L	T	P	C
3	0	0	3

COURSE OBJECTIVES:

- To acquire the fundamental knowledge and to expose to the field of semiconductor theory and devices and their applications.
- To gain adequate understanding of semiconductor device modelling aspects, designing devices for electronic applications
- To acquire the fundamental knowledge of different semiconductor device modelling aspects.

UNIT I MOS CAPACITORS 9

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Nonequilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–OxideInterface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown.

UNIT II MOSFET DEVICES 9

Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET

Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields

UNIT III CMOS DEVICE DESIGN 9

CMOS Scaling, Constant-Field Scaling, Generalized Scaling, Nonscaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Nonuniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements.

UNIT IV BIPOLAR DEVICES 9

n–p–n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Nonideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent

Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor.

UNIT V MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS 9

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of this course, the students will be able to

CO1: Explore the properties of MOS capacitors.

CO2: Analyze the various characteristics of MOSFET devices.

CO3: Describe the various CMOS design parameters and their impact on performance of the device.

CO4: Discuss the device level characteristics of BJT transistors.

CO5: Identify the suitable mathematical technique for simulation.

REFERENCES:

1. Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.
2. A.B. Bhattacharyya “Compact MOSFET Models for VLSI Design”, John Wiley & Sons Ltd, 2009.
3. Ansgar Jungel, “Transport Equations for Semiconductors”, Springer, 2009
4. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd, 2004
5. Selberherr, S., “Analysis and Simulation of Semiconductor Devices”, Springer-Verlag., 1984
6. Behzad Razavi, “Fundamentals of Microelectronics” Wiley Student Edition, 2nd Edition, 2014
7. J P Collinge, C A Collinge, “Physics of Semiconductor devices” Springer, 2002.
8. S.M.Sze, Kwok.K. NG, “Physics of Semiconductor devices”, Springer, 2006.

CO-PO MAPPING:

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	2		1	1		
2	2		1	1		
3	2		2	1		
4	2		1	1		
5	2		2	1	2	
Avg	(10/5)=2		(7/5)=1.4	(5/5)=1	(2/1)=2	

1 - Low, 2 - Medium, 3 - high, ‘-' - No Correlation

24VL101P FPGA LABORATORY L T P C

0 0 4 2

COURSE OBJECTIVES:

- To help engineers read, understand, and maintain digital hardware models and conventional verification test benches written in Verilog and System Verilog.
- To provide a critical language foundation for more advanced training on System Verilog

LIST OF EXPERIMENTS

1. Introduction to Verilog and System Verilog
2. Running simulator and debug tools
3. Experiment with 2 state and 4 state data types
4. Experiment with blocking and non-blocking assignments
5. Model and verify simple ALU
6. Model and verify an Instruction stack
7. Use an interface between testbench and DUT
8. Developing a test program
9. Create a simple and advanced OO testbench
10. Create a scoreboard using dynamic array
11. Use mailboxes for verification
12. Generate constrained random test values
13. Using coverage with constrained random tests

TOTAL: 60 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Understand and use the System Verilog RTL design and synthesis features, including new data types, literals, procedural blocks, statements, and operators, relaxation of Verilog language rules, fixes for synthesis issues, enhancements to tasks and functions, new hierarchy and connectivity features, and interfaces.

CO2: Appreciate and apply the System Verilog verification features, including classes, constrained random stimulus, coverage, strings, queues and dynamic arrays, and learn how to utilize these features for more effective and efficient verification.

CO3: The implementation of higher level of abstraction to design and verification

CO4: Develop Verilog test environments of significant capability and complexity.

CO5: Integrate scoreboards, multichannel sequencers and Register Models

CO-PO MAPPING:

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	1	0	1	1	1	0
2	1	0	1	1	1	0
3	1	0	1	1	1	0
4	1	0	1	1	2	0
5	1	0	1	1	1	0
Avg	(5/5)=1	0	(5/5)=1	(5/5)=1	(6/5)=1.2	0

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

VL4102P ANALOG IC DESIGN LABORATORY L T P C

0 0 4 2

COURSE OBJECTIVES:

- Carry out a detailed analog circuit design starting with transistor characterization and finally realizing an IA design.
- At various stages of design, exposure to state of art CAD VLSI tool in various phases of experiments designed to bring out the key aspects of each important module in the CAD tool including the simulation, layout, LVS and parasitic extracted simulation.

LIST OF EXPERIMENTS

1. Extraction of process parameters of CMOS process transistors
   a. Plot I_D vs. V_{GS} at different drain voltages for NMOS, PMOS.
   b. Plot I_D vs. V_{GS} at particular drain voltage for NMOS, PMOS and determine Vt.
   c. Plot log I_D vs. VGS at particular gate voltage for NMOS, PMOS and determine I_{OFF} and sub- threshold slope.
   d. Plot I_D vs. V_{DS} at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   e. Extract V_{th} of NMOS/PMOS transistors (short channel and long channel). Use V_{DS} of appropriate voltage To extract V_{th} use the following procedure.
   i) Plot g_m vs V_{GS} using SPICE and obtain peak g_m point.
   ii) Plot $y=I_D/(g_m)$ as a function of VGS using SPICE.
   iii) Use SPICE to plot tangent line passing through peak gm point in y (V_{GS}) plane and determine V_{th}.
   a. Plot I_D vs. V_{DS} at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it.
   f. CMOS inverter design and performance analysis
   b. i. Plot VTC curve for CMOS inverter and thereon plot dV_{out} vs. dV_{in} and determine transition voltage and gain g. Calculate V_{IL}, V_{IH}, NM_H, NM_L for the inverter.
   ii. Plot VTC for CMOS inverter with varying V_{DD}.
   iii. Plot VTC for CMOS inverter with varying device ratio.
   c. Perform transient analysis of CMOS inverter with no load and with load and determine propagation delay t_{pHL}, t_{pLH}, 20%-to-80% rise time t_r and 80%-to-20% fall time t_f.

   d. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.

3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.
4. Single stage amplifier design and performance analysis
   a. Plot small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors.
   b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.
      i. Establish a test bench to achieve $V_{DSQ}=V_{DD}/2$.

      ii. Calculate input bias voltage for a given bias current.
      iii. Use spice and obtain the bias current. Compare with the theoretical value
      iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in spice, considering load capacitance.
      v. Plot step response of the amplifier with a specific input pulse amplitude.
      Vi Derive time constant of the output and compare it with the time constant resulted from -3dB Band Width.
      vii. Use spice to determine input voltage range of the amplifier

5. Three OPAMP Instrumentation Amplifier (INA).
   Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
      i. Draw the schematic of op-amp macro model.
      ii. Draw the schematic of INA.
      iii. Obtain parameters of the op-amp macro model such that it meets a given specification for:
      i. low-frequency voltage gain,

ii. unity gain BW (fu),

iii. input capacitance,

iv. output resistance,

v. CMRR

b. Draw schematic diagram of CMRR simulation setup.

c. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).

d. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.

e. Repeat (iii) to (vi) by considering CMRR of all OPAMPs with another low frequency gain setting.

6. Use Layout editor.

a. Draw layout of a minimum size inverter using transistors from CMOS process library. Use Metal 1 as interconnect line between inverters.
b. Run DRC, LVS and RC extraction. Make sure there is no DRC error.
c. Extract the netlist. Use extracted netlist and obtain $t_{PHL}t_{PLH}$ for the inverter using Spice.
d. Use a specific interconnect length and connect and connect three inverters in a chain.
e. Extract the new netlist and obtain t_{PHL} and t_{PLH} of the middle inverter.
f. Compare new values of delay times with corresponding values obtained in part 'c'.

7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter

a. low-frequency voltage gain,
b. unity gain BW (fu),
c. Power dissipation

i. Perform DC analysis and determine input common mode range and compare with the theoretical values.
ii. Perform time domain simulation and verify low frequency gain.
iii. Perform AC analysis and verify.

TOTAL: 60 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Design digital and analog Circuit using CMOS given a design specification.

CO2: Design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors and compute the input/output impedances

CO3: Use EDA tools for Circuit Design

CO-PO MAPPING:

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	1	1	1	1	1	1
2	1	1	1	1	1	1
3	1	1	1	1	1	1
4	1	1	1	1	1	1
5	1	1	1	1	1	1
6	(5/5)=1	(5/5)=1	(5/5)=1	(5/5)=1	(5/5)=1	(5/5)=1

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL201T DESIGN FOR VERIFICATION USING UVM L T P C
3 0 0 3

COURSE OBJECTIVES:

1. To provide the students complete understanding on UVM testing
2. To become proficient at UVM verification,
3. To provide an experience on self checking UVM testbenches

UNIT I INTRODUCTION 9

Overview- The Typical UVM Testbench Architecture- The UVM Class Library-Transaction-Level Modeling (TLM) -Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation

UNIT II DEVELOPING REUSABLE VERIFICATION COMPONENTS 9

Modeling Data Items for Generation - Transaction-Level Components - Creating the Driver - Creating the Sequencer - Connecting the Driver and Sequencer -Creating the Monitor - Instantiating Components- Creating the Agent - Creating the Environment -Enabling Scenario Creation -Managing of Test-Implementing Checks and Coverage

UNIT III UVM USING VERIFICATION COMPONENTS 9

Creating a Top-Level Environment- Instantiating Verification Components - Creating Test Classes -Verification Component Configuration - Creating and Selecting a User-Defined Test - Creating Meaningful Tests- Virtual Sequences- Checking for DUT Correctness- Scoreboards- Implementing a Coverage Model

UNIT IV UVM USING THE REGISTER LAYER CLASSES 9

Using The Register Layer Classes - Back-Door Access -Special Registers -Integrating a Register- Model in a Verification Environment- Integrating a Register Model- Randomizing Field Values- Pre-Defined Sequences

UNIT V ASSIGNMENT IN TESTBENCHES 9

Assignment, APB: Protocol, Test bench Architecture, Driver and Sequencer, Monitor, Agent and Env; Creating Sequences, Building Test, Design and Testing of Top Module.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to

CO1:understand the basic concepts of two methodologies UVM

CO2:build actual verification components.

CO3:generate the register layer classes.

CO4:code testbenches using UVM.

CO5:understand advanced peripheral bus testbenches.

REFERENCES

1. The UVM Primer, An Introduction to the Universal Verification Methodology, Ray Salemi, 2013.
2. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Chris Spear, Greg Tumbush, 3rd edition, 2012.
3. https://www.udemy.com/learn-ovm-UVM
4. http://www.testbench.in/ut_00_index.html
5. http://www.testbench.in/ot_00_index.html

https://www.accellera.org/images/downloads/standards/UVM/UVM_users_guide_1.2.pdf

CO-PO MAPPING:

CO	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
1	1	0	1	1	2	0
2	1	0	1	1	2	0
3	1	0	1	1	2	0
4	1	0	1	1	2	1
5	1	0	1	1	2	1
Avg	(5/5)=1	(0/0)=0	(5/5)=1	(5/5)=1	(10/5)=2	(2/2)=1

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL202T **LOW POWER VLSI DESIGN** **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent methods.
- Identify suitable techniques to reduce the power dissipation.
- Estimate power dissipation of various MOS logic circuits.
- Develop algorithms for low power dissipation.

UNIT I POWER DISSIPATION IN CMOS **9**

Hierarchy of Limits of Power – Sources of Power Consumption – Physics of Power Dissipation in CMOS FET Devices – Basic Principle of Low Power Design.

UNIT II POWER OPTIMIZATION **9**

Logic Level Power Optimization – Circuit Level Low Power Design – Gate Level Low Power Design – Architecture Level Low Power Design – VLSI Subsystem Design of Adders, Multipliers, PLL, Low Power Design

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS **9**

Computer Arithmetic Techniques for Low Power System – Reducing Power Consumption in Combinational Logic, Sequential Logic, Memories – Low Power Clock – Advanced Techniques – Special Techniques, Adiabatic Techniques – Physical Design, Floor Planning, Placement and Routing.

UNIT IV POWER ESTIMATION **9**

Power Estimation Techniques, Circuit Level, Gate Level, Architecture Level, Behavioral Level, – Logic Power Estimation – Simulation Power Analysis –Probabilistic Power Analysis

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER CMOS CIRCUITS **9**

Synthesis for Low Power – Behavioral Level Transform –Algorithms for Low Power – Software Design for Low Power.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students should will be able to:

CO1: able to find the power dissipation of MOS circuits

CO2: design and analyze various MOS logic circuits

CO3 :apply low power techniques for low power dissipation

CO4: able to estimate the power dissipation of ICs

CO5: able to develop algorithms to reduce power dissipation by software tools.

REFERENCES

1. Kaushik Roy and S.C.Prasad, "Low Power CMOS VLSI Circuit Design", Wiley, 2000
2. J.B.Kulo and J.H Lou, "Low Voltage CMOS VLSI Circuits", Wiley 1999.
3. James B.Kulo, Shih-Chia Lin, "Low Voltage SOI CMOS VLSI Devices and Circuits", John Wiley and Sons, Inc. 2001
4. J.Rabaey, "Low Power Design Essentials (Integrated Circuits and Systems)", Springer, 2009

CO-PO MAPPING:

CO	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
1	2	0	2	3	2	0
2	2	0	2	2	2	0
3	1	0	2	2	2	0
4	1	0	2	3	2	0
5	2	0	2	2	3	0
Avg	(8/5)=1.6	(0/0)=0	(10/5)=2	(12/5)=2.4	(11/5)=2.2	(0/0)=0

24VL4203T RFIC DESIGN **L T P C**

3 0 0 3

COURSE OBJECTIVES:

- To study the various impedance matching techniques used in RF circuit design.
- To understand the functional design aspects of LNAs, Mixers, PLLs and VCOs.
- To understand frequency synthesis.

UNIT I IMPEDANCE MATCHING IN AMPLIFIERS **9**

Definition of 'Q', Series Parallel Transformations of Lossy Circuits, Impedance Matching Using 'L', 'Pi' and T Networks, Integrated Inductors, Resistors, Capacitors, Tunable Inductors, Transformers

UNIT II AMPLIFIER DESIGN **9**

Noise Characteristics of MOS Devices, Design of CG LNA and Inductor Degenerated LNAs. Principles of RF Power Amplifiers Design

UNIT III ACTIVE AND PASSIVE MIXERS **9**

Qualitative Description of the Gilbert Mixer - Conversion Gain, and Distortion and Noise , Analysis of Gilbert Mixer – Switching Mixer - Distortion in Unbalanced Switching Mixer -Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - a Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT IV OSCILLATORS **9**

LC Oscillators, Voltage Controlled Oscillators, Ring Oscillators, Delay Cells, Tuning Range in Ring Oscillators, Tuning in LC Oscillators, Tuning Sensitivity, Phase Noise in Oscillators, Sources of Phase Noise

UNIT V PLL AND FREQUENCY SYNTHESIZERS **9**

Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase Noise in PLL, Loop Bandwidth, Basic Integer-N Frequency Synthesizer, Basic Fractional-N Frequency Synthesizer.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Understand the principles of operation of an RF receiver front end.

CO2: Design and apply constraints for LNAs, Mixers and frequency synthesizers.

CO3: Analyze and design mixers.

CO4: Design different types of oscillators and perform noise analysis.

CO5: Design PLL and frequency synthesizer.

REFERENCES

1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998.
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002.
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" Mcgraw-Hill, 1999.
4. Jia-Sheng Hong, "Microstrip Filters for RF/Microwave Applications", Wiley, 2001.
5. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003.

CO-PO MAPPING:

CO	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
1	2	0	2	2	2	0
2	2	0	2	2	2	0
3	1	0	2	2	2	0
4	1	0	2	3	2	0
5	2	0	2	2	2	0
Avg	(8/5)=1.6	(0/0)=0	(10/5)=2	(11/5)=2.2	(10/5)=2	(0/0)=0

24VL204T **VLSI TESTING** **L T P C**

3 0 0 3

COURSE OBJECTIVES:

1. To introduce the VLSI testing.
2. To introduce logic and fault simulation and testability measures
3. To study the test generation for combinational and sequential circuits
4. To study the design for testability.
5. To study the fault diagnosis.

UNIT I INTRODUCTION TO TESTING **9**

Introduction – VLSI Testing Process and Test Equipment – Challenges in VLSI Testing - Test Economics and Product Quality – Fault Modeling – Relationship Among Fault Models.

UNIT II LOGIC & FAULT SIMULATION & TESTABILITY MEASURES **9**

Simulation for Design Verification and Test Evaluation – Modeling Circuits for Simulation – Algorithms for True Value and Fault Simulation – Scoap Controllability and Observability

UNIT III TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS **9**

Algorithms and Representations – Redundancy Identification – Combinational ATPG Algorithms – Sequential ATPG Algorithms – Simulation Based ATPG – Genetic Algorithm Based ATPG.

UNIT IV DESIGN FOR TESTABILITY **9**

Design for Testability Basics – Testability Analysis - Scan Cell Designs – Scan Architecture – Built- in Self-Test – Random Logic Bist – DFT for Other Test Objectives.

UNIT V FAULT DIAGNOSIS **9**

Introduction and Basic Definitions – Fault Models for Diagnosis – Generation of Vectors for Diagnosis – Combinational Logic Diagnosis - Scan Chain Diagnosis – Logic BIST Diagnosis.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Understand VLSI Testing Process.

CO2: Develop Logic Simulation and Fault Simulation .

CO3:Develop Test for Combinational and Sequential Circuits .

CO4: Understand the Design for Testability.

CO5:Perform Fault Diagnosis.

REFERENCES

1. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, “VLSI Test Principles and Architectures”, Elsevier, 2017

2. Michael L. Bushnell and Vishwani D. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits” , Kluwer Academic Publishers, 2017.

3. Niraj K. Jha and Sandeep Gupta, “Testing of Digital Systems”, Cambridge University Press, 2017.

CO-PO MAPPING:

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	2	0	2	3	3	1
2	2	0	2	2	3	1
3	1	0	2	2	3	1
4	1	0	2	3	2	1
5	2	0	2	2	1	1
Avg	(8/5)=1.6	(0/0)=0	(10/5)=2	(12/5)=2.4	(12/5)=2.4	(5/5)=1

1 - Low, 2 - Medium, 3 - high, ‘-' - No Correlation

24VL201P **VERIFICATION USING UVM LABORATORY** **L T P C**
0 0 4 2

COURSE OBJECTIVES:

- To help the engineers to design the system with verilog and system Verilog.
- Complete understanding of Verilog Hardware Description Language.
- To practice for writing synthesizable RTL models that work correctly in both simulation and synthesis.

LIST OF EXPERIMENTS

1. Simulate a simple UVM testbench and DUT
2. Examining the UVM testbench
3. Design and simulate sequence items and sequence
4. Design and simulate a UVM driver and sequencer
5. Design and simulating UVM monitor and agent
6. Design, simulate and examine coverage
7. Design and simulate a UVM scoreboard and environment, and verifying the outputs of a (faulty) DUT
8. Design and simulate a test that runs multiple sequence
9. Design and simulate a configurable UVM test environment

TOTAL: 60 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: understand the features and capabilities of the UVM class library for system Verilog

CO2: combine multiple UVCs into a complete verification environment

CO3:create and configure reusable, scalable, and robust UVM verification components (UVCs)

CO4: create a UVM testbench structure using the UVM library base classes and the UVM factory

CO5:develop a register model for your DUT and use the model for initialization and accessing DUT registers

CO-PO MAPPING:

CO	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
1	1	3	1	1	1	3
2	1	3	1	1	1	3
3	1	3	1	1	1	3
4	1	3	1	1	1	3
5	1	3	1	1	1	3
Avg	(5/5)=1	(15/5)=3	(5/5)=1	(5/5)=1	(5/5)=1	(15/5)=3

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24TM201P TERM PAPER WRITING AND SEMINAR **L T P C**
0 0 2 1

In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps:

1. Selecting a subject, narrowing the subject into a topic
2. Stating an objective.
3. Collecting the relevant bibliography (atleast 15 journal papers)
4. Preparing a working outline.
5. Studying the papers and understanding the authors contributions and critically analysing each paper.
6. Preparing a working outline
7. Linking the papers and preparing a draft of the paper.
8. Preparing conclusions based on the reading of all the papers.
9. Writing the Final Paper and giving final Presentation

Please keep a file where the work carried out by you is maintained. Activities to be carried out

Activity	Instructions	Submission week	Evaluation
Selection of area of interest and Topic Stating an Objective	You are requested to select an area of interest, topic and state an objective	2nd week	**3 %** Based on clarity of thought, current relevance and clarity in writing
Collecting Information about your area & topic	1. List 1 Special Interest Groups or professional society 2. List 2 journals 3. List 2 conferences, symposia or workshops 4. List 1 thesis title 5. List 3 web presences (mailing lists, forums, news sites) 6. List 3 authors who publish regularly in your area Attach a call for papers (CFP) from your area.	3rd week	**3%** (the selected information must be area specific and of international and national standard)
Collection of Journal papers in the topic in the context of the objective – collect 20 & then filter	You have to provide a complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar When picking papers to read - try to: Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them, Favour papers from well-known journals and conferences, Favour "first" or "foundational" papers	4th week	**6%** (the list of standard papers and reason for selection)

	in the field (as indicated in other people's survey paper), Favour more recent papers, Pick a recent survey of the field so you can quickly gain an overview, Find relationships with respect to each other and to your topic area (classification scheme/categorization) Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered		
Reading and notes for first 5 papers	Reading Paper Process For each paper form a Table answering the following questions: What is the main topic of the article? What was/were the main issue(s) the author said they want to discuss? Why did the author claim it was important? How does the work build on other's work, in the author's opinion? What simplifying assumptions does the author claim to be making? What did the author do? How did the author claim they were going to evaluate their work and compare it to others? What did the author say were the limitations of their research? What did the author say were the important directions for future research? Conclude with limitations/issues not addressed by the paper (from the perspective of your survey)	5th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for next 5 papers	Repeat Reading Paper Process	6th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for final 5 papers	Repeat Reading Paper Process	7th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)

Draft outline 1 and Linking papers	Prepare a draft Outline, your survey goals, along with a classification / categorization diagram	8th week	**8%** (this component will be evaluated based on the linking and classification among the papers)
Abstract	Prepare a draft abstract and give a presentation	9th week	**6%** (Clarity, purpose and conclusion) **6%** Presentation & Viva Voce
Introduction Background	Write an introduction and background sections	10th week	**5%** (clarity)
Sections of the paper	Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey	11thweek	**10%** (this component will be evaluated based on the linking and classification among the papers)
Your conclusions	Write your conclusions and future work	12th week	**5%** (conclusions – clarity and your ideas)
Final Draft	Complete the final draft of your paper	13th week	**10%** (formatting, English, Clarity and linking) **4%** Plagiarism Check Report
Seminar	A brief 15 slides on your paper	14th & 15th week	**10%** (based on presentation and Viva-voce)

TOTAL : 60 PERIODS

CO-PO MAPPING:

CO	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
1	1	1	1	1	1	1
2	1	1	1	1	1	1
3	1	1	1	1	1	1
4	1	1	1	1	1	1
5	1	1	1	1	1	1
Avg	(5/5)=1	(5/5)=1	(5/5)=1	(5/5)=1	(5/5)=1	(5/5)=1

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL101E ASIC DESIGN **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- To Focus on the Semi-Custom IC Design and introduces the Principles of Design Logic Cells, I/O Cells and Interconnect Architecture, with Equal Importance given to FPGA and ASIC styles.
- To deal with the entire FPGA and ASIC Design Flow from the Circuit and Layout Design Point of View

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of Asics - Design Flow - CMOS Transistors - Combinational Logic Cell – Sequential Logic Cell - Data

Path Logic Cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical Effort.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti Fuse - Static Ram - EPROM and EEPROM Technology - ACTEL ACT- Xilinx LCA –ALTERA FLEX - ALTERA MAX DC & AC Inputs and Outputs - Clock & Power Inputs - Xilinx I/O Blocks.

UNIT III PROGRAMMABLE ASIC ARCHITECTURE 9

Architecture and Configuration of ARTIX / Cyclone and KINTEX Ultra Scale / STRATIX FPGA – Micro-Blaze / NIOS Based Embedded Systems – Signal Probing Techniques.

UNIT IV LOGIC SYNTHESIS, PLACEMENT AND ROUTING 9

Logic Synthesis - Floor Planning Goals and Objectives, Measurement of Delay in Floor Planning, Floor Planning Tools, I/O and Power Planning, Clock Planning, Placement Algorithms. Routing: Global Routing, Detailed Routing, Special Routing.

UNIT V SYSTEM-ON-CHIP DESIGN 9

SoC Design Flow, Platform-Based and IP Based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High Performance Filters using Delta-Sigma Modulators. Case Studies: Digital Camera, SDRAM, High Speed Data standards.

TOTAL :45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be

CO1: Able to apply Logical Effort Technique for predicting Delay, Delay Minimization and FPGA Architectures.

CO2: Able to Design Logic Cells and I/O Cells.

CO3: Able to analyze the various resources of recent FPGAs.

CO4: Able to use Algorithms for Floor Planning and Placement of Cells and to Apply Routing Algorithms for Optimization of Length and Speed.

CO5: Able to analyze High Performance Algorithms Available for ASICs.

REFERENCES:

1. M.J.S.Smith, "Application Specific Integrated Circuits", Pearson, 2003.
2. Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science,2006
3. Roger Woods, John Mcallister, Dr. Ying Yi, Gaye Lightbod, “FPGA-Based Implementation of Signal Processing Systems”, Wiley, 2008.

CO-PO MAPPING:

CO	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
1	1	0	1	2	3	1
2	1	0	1	2	3	1
3	1	0	1	2	3	1
4	1	0	1	2	3	1
5	1	0	1	2	3	1
Avg	(5/5)=1	(0/0)=0	(5/5)=1	(10/5)=2	(15/5)=3	(5/5)=1

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL102E EMBEDDED SYSTEM DESIGN L T P C
3 0 0 3

COURSE OBJECTIVES:

1. To understand the design challenges in embedded systems.
2. To program the Application Specific Instruction Set Processors.
3. To understand the bus structures and protocols.
4. To model processes using a state – machine model.
5. To design a real time embedded system.

UNIT I EMBEDDED SYSTEM OVERVIEW 9

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Components, Optimizing Custom Single-Purpose Processors.

UNIT II GENERAL AND SINGLE PURPOSE PROCESSOR 9

Basic Architecture, Pipelining, Superscalar and VLIW Architectures, Programmer's View, Development Environment, Application-Specific Instruction-Set Processors (ASIPS) Microcontrollers, Timers, Counters and Watchdog Timer, UART, LCD Controllers and Analog-to- Digital Converters, Memory Concepts.

UNIT III BUS STRUCTURES 9

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus - based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM bus, Wireless Protocols – IRDA, Bluetooth, IEEE 802.11.

UNIT IV STATE MACHINE AND CONCURRENT PROCESS MODELS 9

Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, RTOS – System design using RTOS.

UNIT V SYSTEM DESIGN 9

Burglar alarm system-Design goals -Development strategy-Software development-Relevance to more complex designs- Need for emulation -Digital echo unit-Creating echo and reverb-Design requirements-Designing the codecs -The overall system design

SUGGESTED ACTIVITIES:

1: Do microcontroller based design experiments.

2: Create program –state models for different embedded applications. 3: Design and develop embedded solutions for real world problems.

COURSE OUTCOMES:

CO1: Knowledge of different protocols

CO2: Apply state machine techniques and design process models.

CO3: Apply knowledge of embedded sotware development tools and RTOS

CO4: Apply networking principles in embedded devices.

CO5: Design suitable embedded systems for real world applications.

TOTAL:45 PERIODS

REFERENCES:

1. Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & Sons, 2009.
2. Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.
3. Bruce Powel Douglas, "Real Time UML, Second Edition: Developing Efficient Objects for Embedded Systems", 3rd Edition 2004, Pearson Education
4. Daniel W.Lewis, "Fundamentals of Embedded Software where C and Assembly Meet", Pearson Education, 2004
5. Bruce Powel Douglas, "Real Time UML; Second Edition: Developing Efficient Objects for Embedded Systems", 3rd Edition 1999, Pearson Education.

CO-PO MAPPING:

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	1	0	2	2	3	1
2	1	0	2	2	3	1
3	1	0	2	2	3	1
4	1	0	2	2	3	1
5	1	0	2	2	3	1
Avg	(5/5)=1	(0/0)=0	(10/5)=2	(10/5)=2	(15/5)=3	(5/5)=1

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL103E ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- To gain broad conceptual understanding of the various aspects of electromagnetic (EM) interference and compatibility
- To develop a theoretical understanding of electromagnetic shielding effectiveness
- To understand ways of mitigating EMI by using shielding, grounding and filtering
- To understand the need for standards and to appreciate measurement methods
- To understand how EMI impacts wireless and broadband technologies

UNIT I INTRODUCTION & SOURCES OF EM INTERFERENCE **9**

Introduction - Classification of sources - Natural sources - Man-made sources - Survey of the electromagnetic environment.

UNIT II EM SHIELDING **9**

Introduction - Shielding effectiveness - Far-field sources - Near-field sources - Low-frequency, magnetic field shielding - Effects of apertures

UNIT III INTERFERENCE CONTROL TECHNIQUES **9**

Equipment screening - Cable screening - grounding - Power-line filters - Isolation - Balancing - Signal-line filters - Nonlinear protective devices.

UNIT IV EMC STANDARDS, MEASUREMENTS AND TESTING **9**

Need for standards - The international framework - Human exposure limits to EM fields -EMC measurement techniques - Measurement tools - Test environments.

UNIT V EMC CONSIDERATIONS IN WIRELESS AND BROADBAND TECHNOLOGIES **9**

Efficient use of frequency spectrum - EMC, interoperability and coexistence - Specifications and alliances - Transmission of high-frequency signals over telephone and power networks – EMC and digital subscriber lines - EMC and power line telecommunications.

SUGGESTED ACTIVITIES:

1. Investigate various case studies related to EMIC. Example: Chernobyl Disaster in 1986.
2. Develop some understanding about the design of EM shields in electronic system design and packaging.

COURSE OUTCOMES:

Upon completion of this course, the student will be able to

CO1: Demonstrate knowledge of the various sources of electromagnetic interference

CO2: Display an understanding of the effect of how electromagnetic fields couple through apertures, and solve simple problems based on that understanding

CO3: Explain the EMI mitigation techniques of shielding and grounding

CO4: Explain the need for standards and EMC measurement methods

CO5: Discuss the impact of EMC on wireless and broadband technologies

TOTAL:45 PERIODS

REFERENCES

1. Christopoulos C, Principles and Techniques of Electromagnetic Compatibility, CRC Press, Second Edition, Indian Edition, 2013.
2. Paul C R, Introduction to Electromagnetic Compatibility, Wiley India, Second Edition,2008.
3. Kodali V P, Engineering Electromagnetic Compatibility, Wiley India, Second Edition,2010.
4. Henry W Ott, Electromagnetic Compatibility Engineering, John Wiley & Sons Inc, Newyork,2009.
5. Scott Bennett W, Control and Measurement of Unintentional Electromagnetic Radiation, John Wiley& Sons Inc., Wiley Interscience Series, 1997.

CO-PO MAPPING:

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	2		1	2	1	1
2	3		1	2	1	1
3	2		1	2	1	1
4	2		1	2	1	1
5	2		1	2	1	1
Avg	2.5		1	2	1	1

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL104E **DATA CONVERTERS** **L T P C**
3 0 0 3

COURSE OBJECTIVES:

1. To teach Analog to Digital and Digital to Analog Converters characteristics.
2. To teach the design of Switched Capacitor based Circuits.
3. To teach the design of Analog to Digital and Digital to Analog Converters.

UNIT I INTRODUCTION & CHARACTERISTICS OF AD/DACONVERTER CHARACTERISTICS **9**

Evolution, Types and Applications of AD/DA Converter Characteristics, Issues in Sampling, Quantization and Reconstruction, Oversampling and Anti-aliasing Filters.

UNIT II SWITCH CAPACITOR CIRCUITS AND COMPARATORS **9**

Switched-Capacitor Amplifiers, Switched Capacitor Integrator, Switched Capacitor Common Mode Feedback. Single Stage Amplifier as Comparator, Cascaded Amplifier Stages as Comparator, Latched Comparators. Offset Cancellation, Op Amp Offset Cancellation, Calibration Techniques

UNIT III NYQUIST RATE D/A CONVERTERS **9**

Current Steering DACs, Capacitive DACs, Binary Weighted Vs. Thermometer DACS, Issues in Current Element Matching, Clock Feed Through, Zero Order Hold Circuits, DNL, INL and Other Performance Metrics of ADCs and DACs

9

UNIT IV PIPELINE AND OTHER ADCS

Performance Metrics, Flash Architecture, Pipelined Architecture, Successive Approximation Architecture, Time Interleaved Architecture.

9

UNIT V SIGMA DELTA CONVERTERS

STF, NTF, First Order and Second Order Sigma Delta Modulator Characteristics, Estimating The Maximum Stable Amplitude, CTDSMs, Op amp Nonlinearities

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be

CO1: able to carry out the design calculations for developing the various blocks associated with a typical CMOS AD or DA Converter.

CO2: able to design and implement circuits using Switched Capacitor Concepts

CO3: able to analyze and design D/A Converters

CO4: able to design different types of A/Ds

CO5: able to analyze and design Sigma Delta converter

REFERENCES

1. Behzad Razavi, "Principles of Data Conversion System Design", IEEE Press, 1995.
2. M. Pelgrom, "Analog-to-Digital Conversion", Springer, 2010.
3. Rudy Van De Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters" Kluwer Acedamic Publishers, Boston, 2003.
4. J. G. Proakis, D. G. Manolakis, "Digital Signal Processing Principles, Algorithms and Applications", Prentice Hall, 4th Edition, 2006.
5. Shanthi Pavan, Richard Schreier, Gabor C. Temes , "Understanding Delta-Sigma Data Converters", Willey –IEEE Press, 2nd Edition, 2017.

CO-PO MAPPING:

CO	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
1	1	0	2	2	0	0
2	1	0	2	2	0	0
3	1	0	2	2	0	0
4	1	0	2	2	0	0
5	1	0	2	2	0	0
Avg	(5/5)=1	(0/0)=0	(10/5)=2	(10/5)=2	(0/0)=0	(0/0)=0

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL105E HARDWARE SOFTWARE CO-DESIGN FOR FPGA

L	**T**	**P**	**C**
3	**0**	**0**	**3**

Course Objectives:

1 To acquire the knowledge about system specification and modelling

2 To learn the formulation of partitioning

3 To study the different technical aspects about prototyping and emulation

UNIT I SYSTEM SPECIFICATION AND MODELLING **9**

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling, Co-Design for Heterogeneous Implementation - Processor Synthesis, Single-Processor Architectures with One ASIC, Single-Processor

Architectures with Many ASICs, Multi-Processor Architectures, Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification

UNIT II HARDWARE/SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of The Partitioning Graph, Formulation of The HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based On Genetic Algorithms.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data- Dominated Systems, Mixed Systems and Less Specialized Systems.

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-Simulation

TOTAL: 45 PERIODS

COURSE OUTCOMES: At the end of this course, the students will be able to

CO1	Describe The Broad Range of System Architectures and Design Methodologies that currently exist and define their fundamental attributes.
CO2	Discuss the Dataflow Models as a State-of-the-Art Methodology to Solve Co-Design Problems and to Optimize the balance between Software and Hardware.
CO3	Understand in Translating between Software and Hardware Descriptions through Co-Design Methodologies.
CO4	Understand the State-of-The-Art practices in developing Co-Design Solutions to problems using modern Hardware/Software Tools for building prototypes..
CO5	Understand the Concurrent Specification from an Algorithm, Analyze its behavior and partition the Specification into Software (C Code) and Hardware (HDL) Components.

REFERENCES:

1	Patrick Schaumont, "A Practical Introduction to Hardware/Software Co-design", Springer,2010.
2	Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Publisher, 1998.
3	Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice", Kluwer Academic Publisher,1997.
4	Giovanni De Micheli, Rolf Ernst Morgon, "Reading in Hardware/Software Co-Design", Kaufmann Publisher,2001.

CO-PO MAPPING:

CO	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
1	1	0	2	2	0	0
2	1	0	2	2	0	0
3	1	0	2	2	0	0
4	1	0	2	2	2	0
5	1	0	2	2	2	0
Avg	(5/5)=1	(0/0)=0	(10/5)=2	(10/5)=2	(4/5)=0.8	(0/0)=0

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL106E	PATTERN RECOGNITION	L	T	P	C
		3	0	0	3

Course Objectives

1. Understand the in-depth concept of Pattern Recognition
2. Implement Bayes Decision Theory
3. Understand the in-depth concept of Perception and related Concepts
4. Understand the concept of ML Pattern Classification
5. Understand the concept of DL Pattern Recognition

UNIT I PATTERN RECOGNITION 9

Induction Algorithms. Rule Induction. Decision Trees. BayesianMethods. Overview. NaiveBayes. The Basic Na¨ıve Bayes Classifier. Naive Bayes Induction for Numeric Attributes. Correction to the Probability Estimation. Laplace Correction. No Match. Other Bayesian Methods. Other Induction Methods. Neural Networks. Genetic Algorithms. Instance-based Learning. Support Vector Machines.

UNIT II STATISTICAL PATTERN RECOGNITION 9

About Statistical Pattern Recognition. Classification and regression. Features, Feature Vectors, and Classifiers. Pre-processing and feature extraction. The curse of dimensionality. Polynomial curve fitting. Model complexity. Multivariate non-linear functions. Bayes' theorem. Decision boundaries. Parametric methods. Sequential parameter estimation. Linear discriminant functions. Fisher's linear discriminant. Feed-forward network mappings.

UNIT III BAYES DECISION THEORY CLASSIFIERS 9

Bayes Decision Theory. Discriminant Functions and Decision Surfaces. The Gaussian Probability Density Function. The Bayesian Classifier for Normally Distributed Classes. Exact interpolation. Radial basis function networks. Network training. Regularization theory. Noisy interpolation theory. Relation to kernel regression. Radial basis function networks for classification. Comparison with the multi-layer perceptron. Basis function optimization.

UNIT IV LINEAR DISCRIMINANT FUNCTIONS 9

Linear Discriminant Functions and Decision Surfaces. The Two-Category Case. The Multicategory Case. The Perceptron Criterion Function. Batch Perceptron. Perceptron Algorithm Convergence. The Pocket Algorithm. Mean Square Error Estimation. Stochastic Approximation and the LMS Algorithm. Convergence Proof for Single-Sample Correction. Fixed increment descent. Some Direct Generalizations. Fixed increment descent. Batch variable increment Perceptron. Balanced Winnow algorithm. Relaxation Procedures. The Descent Algorithm

UNIT V NONLINEAR CLASSIFIERS 9

The Two Layer Perception. The Three Layer Perception. Algorithms Based On Exact Classification Of The Training Set. Feedforward operation and classification. General feedforward operation. Expressive power of multilayer networks. Backpropagation algorithm. Network learning. Training protocols. Stochastic Backpropagation. Batch Backpropagation. Radial basis function networks (RBF). Special bases. Time delay neural networks (TDNN). Recurrent networks. Counter propagation. Cascade-Correlation. Cascade-correlation. Neocognitron

TOTAL: 45 PERIODS

SUGGESTED ACTIVITIES:

1. Car Sales Pattern Classification using Support Vector Classifier
2. Avocado Sales Pattern Recognition using Linear regression
3. Tracking Movements by implementing Pattern Recognition
4. Detecting Lanes by implementing Pattern Recognition
5. Pattern Detection in SAR Images

COURSE OUTCOMES:

- **CO1** Discover imaging, and interpretation of temporal patterns
- **CO2** Identify Structural Data Patterns

CO3	Implement Pattern Classification using Machine Learning Classifiers
CO4	Implement Pattern Recognition using Deep Learning Models
CO5	Implement Image Pattern Recognition

REFERENCES:

1 Pattern Classification, 2nd Edition, Richard O. Duda, Peter E. Hart, and David G. Stork. Wiley, 2000

2 Pattern Recognition, Jürgen Beyerer, Matthias Richter, and Matthias Nagel. 2018

3 Pattern Recognition and Machine Learning, Christopher M. Bishop. Springer, 2010

4 Pattern Recognition and Classification, Dougherty, and Geoff. Springer, 2013

5 Practical Machine Learning and Image Processing, Himanshu Singh. Apress, 2019

CO-PO Mapping:

CO	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
1	3		2	3	1	1
2	3		2	3	1	1
3	3		2	3	1	1
4	3		2	3	1	1
5	3		2	3	1	1
Avg	(15/5)=3		(10/5)=2	(15/5)=3	(5/5)=1	(5/5)=1

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL201E DSP STRUCTURES FOR VLSI

L	**T**	**P**	**C**
3	**0**	**0**	**3**

Course Objectives

1 To understand the fundamentals of DSP

2 To learn various DSP structures and their implementation.

3 To know designing constraints of various filters

4 Design and optimize VLSI architectures for basic DSP algorithms

5 To enable students to design VLSI system with high speed and low power.

UNIT I INTRODUCTION TO DIGITAL SIGNAL PROCESSING 9

Linear system theory- convolution- correlation - DFT- FFT- basic concepts in FIR filters and IIR filters- filter realizations. Representations of DSP algorithms- block diagram-SFG-DFG.

UNIT II ITERATION BOUND, PIPELINING AND PARALLEL PROCESSING OF FIR FILTER 9

Data-flow graph representations- Loop bound and Iteration bound algorithms for computing iteration bound-LPM algorithm. Pipelining and parallel processing: pipelining of FIR digital filters- parallel processing, pipelining and parallel processing for low power.

UNIT III RETIMING, UNFOLDING AND FOLDING 9

Retiming: definitions, properties and problems- solving systems of inequalities. Properties of Unfolding, critical path, Unfolding and Retiming, applications of Unfolding, Folding transformation- register minimization techniques, register minimization in folded architecture- folding of multirate system.

UNIT IV FAST CONVOLUTION 9

Cook-toom algorithm- modified cook-Toom algorithm. Design of fast convolution algorithm by inspection - Winograd algorithm- modified Winograd algorithm

UNIT V ARITHMETIC STRENGTH REDUCTION IN FILTERS 9

Parallel FIR filters-fast FIR algorithms-two parallel and three parallel. Parallel architectures for rank order filters -odd-even, merge-sort architecture-rank order filter architecture-parallel rank order filters-running order merge order sorter, low power rank order filter.

TOTAL: 45 PERIODS

COURSE OUTCOMES: At the end of the course student will be able

CO1 Acquired knowledge about fundamentals of DSP processors.

CO2 Improve the overall performance of DSP system through various transformation and optimization techniques.

CO3 To understand the need of different types of instructions for DSP..

CO4 Optimize design in terms of computation complexity and speed.

CO5 Understand clock based issues and design asynchronous and wave pipelined systems**.**

REFERENCES:

1 K.K Parhi: "VLSI Digital Signal Processing", John-Wiley, 2nd Edition Reprint, 2008.

2 John G.Proakis, Dimitris G.Manolakis, "Digital Signal Processing", Prentice Hall of India, 1st Edition, 2009.

CO-PO MAPPING:

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	1	0	1	1	0	0
2	1	0	1	1	0	0
3	1	0	1	1	0	0
4	1	0	1	1	0	0
5	1	0	1	1	0	0
Avg	(5/5)=1	(0/0)=0	(5/5)=1	(5/5)=1	(0/0)=0	(0/0)=0

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL202E POWER MANAGEMENT AND CLOCK DISTRIBUTION CIRCUITS

L	T	P	C
3	0	0	3

Course Objectives:

1 To design ~~of~~ reference circuits and low dropout regulators for desired specifications

2 To understand oscillators choice and requirements for clock generation circuits

3 To design clock generation and recovery in the context of high speed systems

UNIT I VOLTAGE AND CURRENT REFERENCES 9

Current mirrors, self biased current reference, startup circuits, VBE based current reference, VT based current reference, band gap reference , supply independent biasing, temperature independent biasing, PTAT current generation, constant Gm biasing.

UNIT II LOW DROP OUT REGULATORS 9

Analog building blocks, negative feedback, performance metrics, AC design, stability, internal and external compensation, PSRR – internal and external compensation circuits

UNIT III OSCILLATOR FUNDAMENTALS 9

General considerations, ring oscillators, LC oscillators, Colpitts oscillator, jitter and phase noise in ring oscillators, impulse sensitivity function for LC & ring oscillators, phase noise in differential LC oscillators.

UNIT IV CLOCK DISTRIBUTION CIRCUITS 9

PLL fundamental, PLL stability, noise performance, charge-pump PLL topology, CPPLL building blocks, jitter and phase noise performance, DLL fundamentals.

UNIT V CLOCK AND DATA RECOVERY CIRCUITS 9

CDR architectures, transimpedance amplifiers and limiters, CMOS interface, linear half rate CMOS CDR circuits, wide capture range CDR circuits.

TOTAL: 45 PERIODS

COURSE OUTCOMES: At the end of this course, the students will be able to:

CO1 Design band gap reference circuits and low drop out regulator for a given specification.

CO2 Understand specification related to supply and clock generation circuits of IC

CO3 Choose oscillator topology and design meeting the requirement of clock generation circuits.

CO4 Design clock generation circuits in the context of high speed I/Os, high speed broad band communication circuits and data conversion circuits.

CO5 Design clock distribution circuits

REFERENCES:

1 Gabriel.a. Rincon-Mora, "Voltage References from Diode to Precision Higher Order Band gap circuits", John Wiley & Sons Inc, 2002.

2 Gabriel.a. Rincon-Mora, "Analog IC Design with Low-Dropout Regulators", Mcgraw Hill Professional Pub, 2009.

3 Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata Mcgraw Hill, 2001

4 Floyd M. Gardner ,"Phase Lock Techniques" John Wiley& Sons, Inc 2005.

5 Michiel Steyaert, Arthur H.M. Van Roermund, Herman Casier, "Analog Circuit Design: High Speed Clock and Data Recovery, High-Performance Amplifiers Power Management", Springer, 2008.

6 Behzadrazavi, "Design of Integrated Circuits for Optical Communications", McGraw Hill, 2003.

CO-PO MAPPING

CO	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
1	1	0	2	2	0	0
2	1	0	2	2	0	0
3	1	0	2	2	0	0
4	1	0	2	2	0	0
5	1	0	2	2	0	0
Avg	(5/5)=1	(0/0)=0	(10/5)=2	(10/5)=2	(0/0)=0	(0/0)=0

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL203E RECONFIGURABLE ARCHITECTURES

L	**T**	**P**	**C**
3	**0**	**0**	**3**

Course Objectives:

1 The student shall develop an overview and deeper insight into the research and development that is underway to meet future needs of flexible processors

2 to learn the concepts of implementation, synthesis and placement of modules in reconfigurable architectures

3	to understand the communication techniques and System on Programmable Chip for reconfigurable architectures
4	to learn the process of reconfiguration management
5	to familiarize the applications of reconfigurable architectures

UNIT I INTRODUCTION 9

General purpose computing – domain specific processors – Application Specific Processors – reconfigurable computing – fields of application – evolution of reconfigurable systems – simple Programmable Logic Devices – Complex Programmable Logic Devices – Field Programmable Gate Arrays – coarse grained reconfigurable devices

UNIT II IMPLEMENTATION, SYNTHESIS AND PLACEMENT 9

Integration – FPGA design flow – logic synthesis – LUT based technology mapping – modeling – temporal partitioning algorithms – offline and online temporal placement – managing device's free and occupied spaces.

UNIT III COMMUNICATION AND SOPC 9

Direct communication – communication over third party – bus based communication – circuit switching – Network on Chip – dynamic Network on Chip – System on a Programmable Chip – adaptive multi-processing on chip.

UNIT IV RECONFIGURATION MANAGEMENT 9

Reconfiguration – configuration architectures – managing the reconfiguration process – reducing configuration transfer time – configuration security

UNIT V APPLICATIONS 9

FPGA based parallel pattern matching - low power FPGA based architecture for microphone arrays in Wireless Sensor Networks - exploiting partial reconfiguration on a dynamic coarse grained reconfigurable architecture – parallel pipelined OFDM baseband modulator with dynamic
frequency scaling for 5G systems.

TOTAL: 45 PERIODS

COURSE OUTCOMES: At the end of this course, the students will be able to:

CO1	Analyze the different architecture principles relevant to reconfigurable computing systems
CO2	Compare the tradeoffs that are necessary to meet the area, power and timing criteria of reconfigurable systems
CO3	Analyze the algorithms related to placement and partitioning
CO4	Analyze the communication techniques and system on programmable chip for reconfigurable architectures
CO5	Analyze the principles of Network and System on a Programmable Chip

REFERENCES:

1	Christophe Bobda, "Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications", Springer 2007.
2	Scott Hauck and Andre Dehon, "Reconfigurable Computing: The Theory and Practice of FPGA Based Computation", Elsevier 2008
3	M. Gokhale and P. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", Springer, 2005.
4	Nikoloas Voros Et Al. "Applied Reconfigurable Computing: Architectures, Tools and Applications" Springer, 2018.
5	Koen Bertels, João M.P. Cardoso, Stamatis Vassiliadis, "Reconfigurable Computing: Architectures and Applications", Springer 2006.

CO-PO MAPPING:

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	1	0	2	1	0	0
2	2	0	2	2	0	0
3	1	0	2	1	0	0
4	1	0	2	1	0	0
5	1	0	2	1	0	0
Avg	(6/5)=1.2	(0/0)=0	(10/5)=2	(6/5)=1.2	(0/0)=0	(0/0)=0

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL204E ADVANCED WIRELESS SENSOR NETWORKS

L	T	P	C
3	0	0	3

Course Objectives:

1. To enable the student to understand the role of sensors and the networking of sensed data for different applications.
2. To expose the students to the sensor node essentials and the architectural details, the medium access and routing issues and the energy constrained operational scenario.
3. To enable the student to understand the challenges in synchronization and localization of sensor nodes, topology management for effective and sustained communication, data management and security aspects

UNIT I OVERVIEW OF WIRELESS SENSOR NETWORKS 9

Challenges for wireless sensor networks-characteristics requirements-required mechanisms, difference between mobile ad-hoc and sensor networks, applications of sensor networks- case study, enabling technologies for wireless sensor networks.

UNIT II ARCHITECTURES 9

Single-node architecture - hardware components, energy consumption of sensor nodes , operating systems and execution environments, network architecture - sensor network scenarios, optimization goals and figures of merit, gateway concepts. Physical layer and transceiver design considerations.

UNIT III MAC AND ROUTING 9

MAC protocols for wireless sensor networks, IEEE 802.15.4, Zigbee, low duty cycle protocols and wakeup concepts - s-MAC , the mediation device protocol, wakeup radio concepts, address and name management, assignment of MAC addresses, routing protocols- energy- efficient routing, geographic routing.

UNIT IV INFRASTRUCTURE ESTABLISHMENT 9

Topology control, clustering, time synchronization, localization and positioning, sensor tasking and control.

UNIT V DATA MANAGEMENT AND SECURITY 9

Data management in WSN, storage and indexing in sensor networks, query processing in sensor, data aggregation, directed diffusion, tiny aggregation, greedy aggregation, security in WSN, security protocols for sensor networks, secure charging and rewarding scheme, secure event and
event boundary detection.

45 PERIODS

COURSE OUTCOMES: At the end of this course, the students will be able to:

- **CO1** design and implement simple wireless network concepts
- **CO2** design, analyze and implement different network architectures
- **CO3** implement MAC layer and routing protocols
- **CO4** deal with timing and control issues in wireless sensor networks
- **CO5** analyze and design secured wireless sensor networks

REFERENCES:

1 Holger Karl & Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks" , John Wiley, 2005.

2 Erdal Çayirci , Chunming Rong, "Security in Wireless Ad Hoc and Sensor Networks", John Wiley and Sons, 2009.

3 Kazem Sohraby, Daniel Minoli, & Taieb Znati, "Wireless Sensor Networks-S Technology, Protocols, and Applications", John Wiley, 2007

4 Yingshu Li, My T. Thai,Weili Wu, "Wireless Sensor Networks and Applications", Springer, 2008.

CO-PO MAPPING :

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	0	0	3	1	3	0
2	0	0	2	1	3	0
3	3	0	1	1	3	0
4	3	0	2	1	0	0
5	3	0	2	1	3	0
Avg	(9/3)=3	(0/0)=0	(10/5)=2	(5/5)=1	(12/4)=3	(0/0)=0

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL205E SIGNAL INTEGRITY FOR HIGH-SPEED DESIGN

L	T	P	C
3	0	0	3

Course Objectives

1 To identify sources affecting the speed of digital circuits.

2 To introduce methods to improve the signal transmission characteristics

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossless models.

UNIT III NON-IDEAL EFFECTS 9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors.

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic

,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis.

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

45 PERIODS

COURSE OUTCOMES: At the end of this course, the students will be able to:

CO1	identify sources affecting the speed of digital circuits.
CO2	identify methods to improve the signal transmission characteristics
CO3	characterise and model multiconductor transmission line
CO4	analyse clock distribution system and understand its design parameters
CO5	analyse nonideal effects of transmission line

REFERENCES:

1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR , 2003.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handboo of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.
4. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.

TOOLS REQUIRED:

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2. HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html
3. SPECTRAQUEST from Cadence, http://www.specctraquest.com or any equivalent open source tool

CO-PO MAPPING:

CO	POs					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
1	1	0	2	3	1	0
2	1	0	2	3	1	0
3	1	0	2	3	1	0
4	1	0	2	1	1	0
5	1	0	2	1	1	0
Avg	(5/5)=1	(0/0)=0	(10/5)=2	(11/5)=2.2	(5/5)=1	(0/0)=0

1 - Low, 2 - Medium, 3 - high, '-' - No Correlation

24VL206E **SYSTEM ON CHIP** **L T P C**

3 0 0 3

Course Objectives:

1. To introduce architecture and design concepts underlying system on chips.
2. Students can gain knowledge of designing SoCs.
3. To impart knowledge about the hardware-software design of a modest complexity chip allthe way from specifications, modeling, synthesis and physical design.

UNIT I **SYSTEM ARCHITECTURE: OVERVIEW** **9**

Components of the system – Processor architectures – Memory and addressing – system levelinterconnection – SoC design requirements and specifications – design integration – design complexity – cycle time, die area and cost, ideal and practical

scaling, area-time-power tradeoff in processor design, Configurability.

UNIT II PROCESSOR SELECTION FOR SOC 9

Overview – soft processors, processor core selection. Basic concepts – instruction set, branches, interrupts and exceptions. Basic elements in instruction handling – Minimizing pipeline delays – reducing the cost of branches – Robust processors – Vector processors, VLIW processors, Superscalar processors.

UNIT III MEMORY DESIGN 9

SoC external memory, SoC internal memory, Scratch pads and cache memory – cache organization and write policies – strategies for line replacement at miss time – split I- and Dcaches – multilevel caches – SoC memory systems – board based memory systems – simpleprocessor/memory interaction.

UNIT IV INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION 9

Bus architectures – SoC standard buses – AMBA, CoreConnect – Processor customization approaches – Reconfigurable technologies – mapping designs onto reconfigurable devices - FPGA based design – Architecture of FPGA, FPGA interconnect technology, FPGA memory, Floor plan and routing.

UNIT V FPGA BASED EMBEDDED PROCESSOR 9

Hardware software task partitioning – FPGA fabric Immersed Processors – Soft Processors andHard Processors – Tool flow for Hardware/Software Co-design –Interfacing Processor with memory and peripherals – Types of On-chip interfaces – Wishbone interface, Avalon Switch Matrix, OPB Bus Interface, Creating a Customized Microcontroller - FPGA-based Signal Interfacing and Conditioning.

45 PERIODS

COURSE OUTCOMES: Upon successful completion of the program the students shall

CO1 Explain all important components of a System-on-Chip and an embedded system, i.e.

CO2 digital hardware and embedded software;

CO3 Outline the major design flows for digital hardware and embedded software;

CO4 Discuss the major architectures and trade-offs concerning performance, cost and power

CO5 consumption of single chip and embedded systems;

REFERENCES:

1 Wayne Wolf, “Modern VLSI Design – System – on – Chip Design”, Prentice Hall, 3rd Edition, 2008.

2 Wayne Wolf , “Modern VLSI Design – IP based Design”, Prentice Hall, 4th Edition, 2008

CO-PO MAPPING:

CO	POs					
	PO1	PO2	PO3	PO4	PO5	PO6
1	1	0	2	1	0	0
2	1	0	2	1	0	0
3	1	0	2	1	0	0
4	1	0	2	1	0	0
5	1	0	2	1	0	0
Avg	(5/5)=1	(0/0)=0	(10/5)=2	(5/5)=1	(0/0)=0	(0/0)=0